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A Review On Multiplier Architecture And Optimization

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Abstract-In arithmetic operation, Multiplier plays an important role in DSP, VLSI, Microprocessor, Microcontroller, IC and SOC. Multiplier logic is observed to be an interior part to perform a numerical task. However, designing a Multiplier for any Integrated circuits or DSP application leads to power dissipation and low speed. To overcome this critical part, Different techniques are implemented to increase multiplier speed, reduce power consumption, delay, area, and computation time. This paper, review on the development of different multiplier architecture, adder, and optimize area in usage level.

I. INTRODUCTION

Multiplication is crucial for Graphic engines Microprocessor, Microcontroller, digital signal processing and Process controllers. In Digital signal processing, multiplier involves in FFR, FIR, Digital communication, spectral analysis, and CMOS full adder circuit. Multiplication operations are primarily shift and add performance. Multiplier is hardware exhaustive and fast. In design of processing unit, the interior function of block performance on input data is the arithmetic and logical units. In arithmetic unit the integral performance are Addition, Subtraction, Multiplication, and Division. Designing a multiplier in integrated circuit leads to lower dissipation and large resource in higher area coverage. To overcome this issue, there are lots of new multiplier architecture to increase speed in Multiplier and adder technique. By using this technique to decrease the number of partial product, delay, number of slices, and number of transistor gate.

II. MODELING DIFFERENT ARCHITECTURE UNIT

The benefit of DSP has become universal and provides broad advantage in various real time implementations. The addition and multiplication of two binary numbers are fundamental and most often using mathematical process in microcontroller, digital signal processing, specific microcircuit. Designing multipliers that are regular in layout, high speed, minimize power, are considerable. These are achieving by using different multiplier. There are Array multiplier, Wallace tree structure, Dada multiplier, Braun multiplier, and modified booth recorder to increase their speed and less power. Some of the adder are also used this technique to minimize area, delay and computation time .There are parallel prefix adder, ripple carry adder, carry propagation adder, kogge stone adder, carry look ahead adder, carry select adder, carry save adder. These are implemented by three method, generation, accumulation and final methods are obtained result, Figure 1. Shows the multiplier architecture

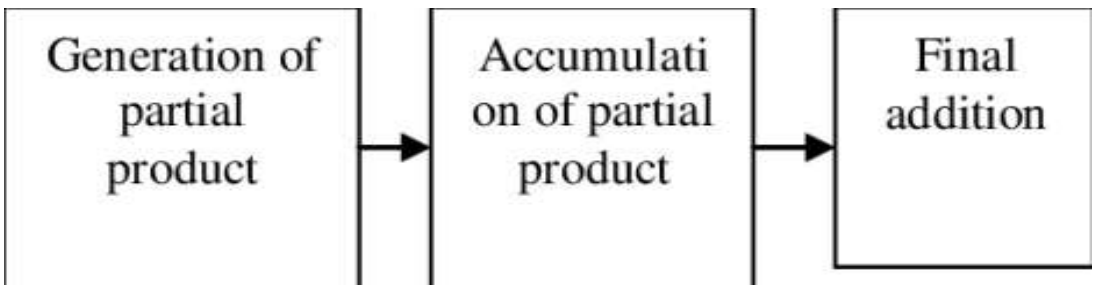

Figure 1. Block diagram for multiplier architecture

1. In Wallace tree multiplier [1] Reduction method is using by 4:2 and 5:2 compressor to minimize the number of partial product and then final stages are implemented by using Sklansky added. It's reducing the minimal depth and high fan out nodes. These are implemented by using TANNER EDA tool in CMOS technology. In Wallace tree multiplier [2] it is a comparison of Normal Wallace tree

structure and reduced complexity Wallace tree structure. In both techniques, there are three stages. The initial stage is partial product generation, second stage is partial product reduction is used by carry skip adder and then final stages are implemented by using parallel prefix adder that is kogge stone adder and Sklansky adder to bring down the number of stages, to improve high speed and low power. By comparing these two techniques the reduced complexity Wallace tree structure is least delay when compared to other normal Wallace tree structure. These are implemented by using Xilinx ISE 9.1 software considering Spartan-3 devices. In booth recording [3] the partial product technique is modified HPM and Dadda compression, to minimize number of stages, and better compression ratio. But it's produce delay and high computation time. These are verified by using cadence design simulator and synthesized using encounter RTL complier from cadence EDA with TSMC 90nm CMOS standard cell library. In 32*32 booth recorder Wallace tree multiplier [4] the partial product generation used by 4:2, 3:2, 5:2 compressor and then final stages are carry select adder. It's produce high speed, but number of bits is increase and produce delay. This process is designed by using Verilog HDL and synthesized for Xilinx vertex 6 FPGA devices. In fixed width booth multiplier [5] the partial product generation by using booth encoder with universal gate and accumulates the partial product frequently to reduce area, delay, and number of slices. Modified booth multiplier with universal gates is better when compared to conventional booth multiplier. These are implemented by using Xilinx IES 12.1 and Spartan device. Adaptive conditional probability estimator [6] is used for booth multiplication to reduce power and achieve high accuracy and truncation error is also obtained. To overcome this truncation error, the booth multiplier is used to two dimensional discrete cosine transform to reduce error and cost but its needs more computation time. In multiplier architecture [7] the multiplier and multiplicand are performed by using reduced spurious transition activity technique and apply with modified booth recorder to reduce a switching power. The detection logic circuit using register is also present to control the latch, carry, and sign extension. This technique is better when compared with CMOS technology. These are implemented by using models from mentor graphics. In Wallace tree multiplier [8] the initial stage by using 4:2 and 5:2 compressor, and partial product accumulation by using carry select adder to minimize the number of stages and raise the amount of speed, but the computation time is high. This simulation has been carried out using Models and Xilinx tool.

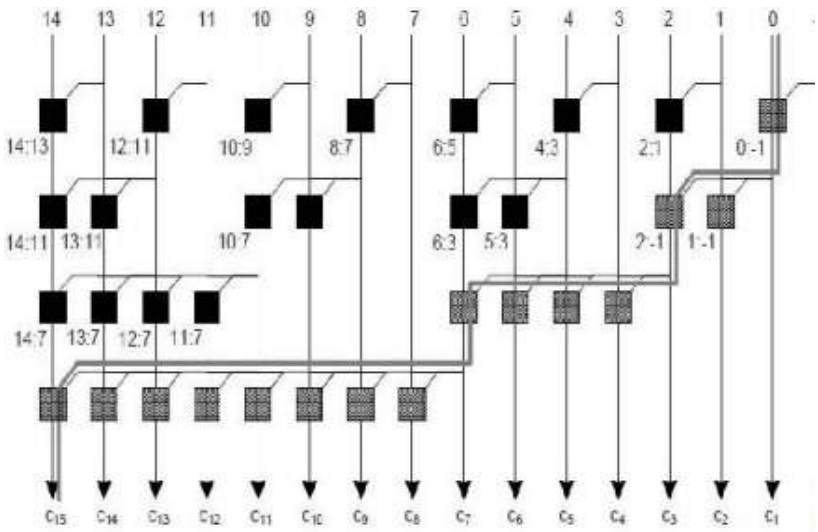

Figure 2. 16 Bit Sklansky Adder

In 16*16 multiplier [9] the partial product are generated by using booth encoded and partial product accumulates by using two technique, first and second stages are performed by using radix 4 booth algorithm with 4:2 compressor, and SQRT CSAL second stages is modified SQRT CSAL. Both process are wont to minimize number of stages, area, logic gates, But it's increase the amount of slices and computation time. This process is synthesized and simulated using Xilinx ISE 12.1. In RCW multiplier [10] the partial product reduction by using energy efficient CMOS full adder to less the number of transistor count and number of slices. But it's produce high power consumption and computation time. In wallace tree structure [11] it is an comparison of conventional wallace tree structure and wallace tree structure with Sklansky adder it's have four stages first stages is 5:2 compressor, second stages is 4:2 compressor, third stage is 3:2 compressor and

then final stages are implemented by using Sklansky added. In both technique, Wallace tree structure with Sklansky adder is better improvement in delay, memory, slices, and latches compare with conventional Wallace tree structure. To minimize memory, low power consumption, latency. In multiplier architecture [12] the initial stages by using booth encoder, accumulates by using Wallace tree with 4:2, 3:2 compressor and then final stages are implemented by using carry look ahead adder to improve speed and minimize delay, number of slices. But its needs high computation time. These are implemented by using Xilinx XC2s 100 FPGA, Figure 2 shows the 16 Bit Sklansky Adder

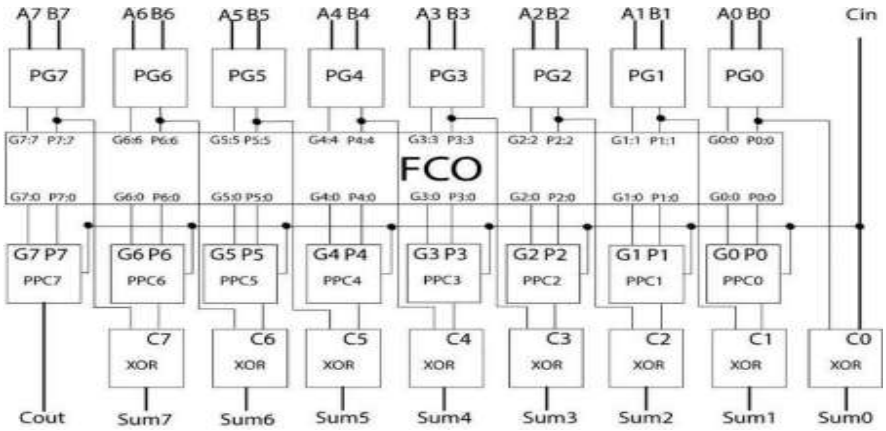

Figure 3. 8 Bit Kogge Stone Adder

In 32*32 bit booth encoded [13] bits are summed by using 4:2, 5:2 and 3:2 in wallace tree structure to minimize the number of partial adder and minimum delay, low power consumption. These are performed by Verilog code. In multiplier architecture [14] partial product generation and accumulation by using modified Wallace tree structure with new bit width aware, carry in prediction logic is used, to lesser the number of stages. By using these technique it's reduce delay and minimize transistor gate. These are implemented by using cadence RTC compiler for 45nm. In 4*4 Vedic multiplier [15] the multiplicand and multiplier are performed by using Vedic multiplier with ripple carry adder to obtain the final result. This is also implemented by using full adder and half adder. To minimize number of slices bonded input, output and delay. But it's very complex while doing 8 bit or 16 bit multiplier and needs more computation time, Figure 3. shows the 8 Bit Kogge Stone Adder.

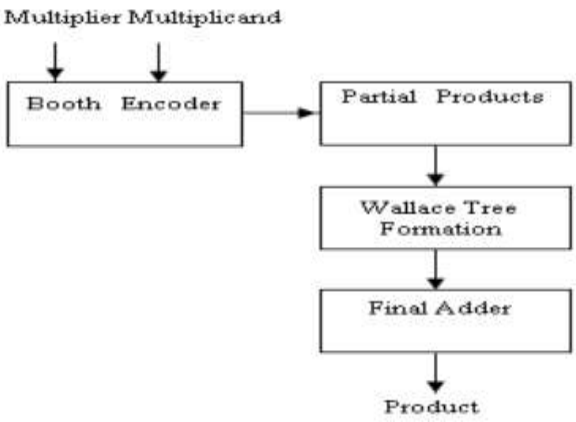

Figure 4. Modified Booth Recorder

In approximate number eight booth number [16] have four stages area unit number encoder, partial product generation, partial product accumulator and so final stages area unit enforced by exploitation Wallace tree structure to lesser the quantity of stages and electronic transistor count. However it's desires high power to accumulate the method. In multiplier architecture [17] the partial product generation and accumulation by using fixed width booth encoded and carry select adder to minimize the number of stages, increase speed. But the truncation error method is produce delay, and high computation time. These are implemented by using

cadence RTL compiler. In changed full adder [18] victimization multiplexers and XOR gate to cut back the facility consumption within the addition circuit, then the ultimate full adder is enforced by victimization Wallace tree structure, to cut back the amount of partial product ,stages and significant path delay, however it's scale back speed of the circuit and high power consumption. These are enforced by victimization Synopsys style compiler victimization SAED ninety nm CMOS technology. In multiplier architecture [19] hybrid 1 bit full adders is applied with CMOS and carry propagation delay to increase speed, less delay and regular layout area, but its produce more computation time. These are implemented by using standard cadence virtuoso tools with 180/90nm technology. In energy efficient high speed wallace tree multiplier [20] the partial product generation by using booth encoding with 3:2, 4:2, 5:2 compressor and final stages are accumulated by using carry save adder to increase amount of transistor count, minimize number of partial products. The comparison of energy efficient high speed Wallace tree structure is better than the other Wallace tree structure, because its measure correct accuracy and minimize the number of slices. Figure 4. Shows the Modified Booth Recorder.

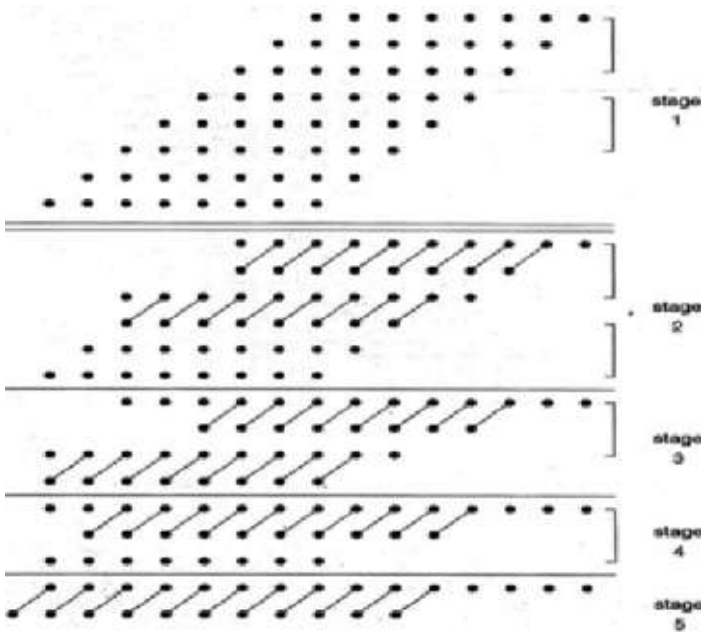

Figure 5. 8 bit wallace tree structure

In Fused add multiplier [21] using modified booth and 4:2 compressor in Wallace tree multiplier and then final stages are implemented by using either Kogge stone adder or Ripple carry adder to increase speed, low power, Figure 5.shows the 8 bit wallace tree structure But its needs more multiplication and high computation time. These are implemented by using Models SE and Xilinx ISE for performance analysis. In DSP architecture [22] it is based on three stages on node data aggregation, parallel prefix operation and folder tree. In folder tree architecture by using kogge stone adder. It is a comparison of folded tree architecture by using kogge stone adder is reduced number of slices, LUT, IOB, and computation time and remove memory bottleneck when compared with unfolded tree architecture by using kogge stone adder. In multiplier architecture [23] the partial product reduction by using 4:2 compressor with both half and full adder then finally the partial product accumulates by using kogge stone adder. These techniques bring down the number of stages, minimized delay, to improve high speed, but the kogge stone adder is very complex and its need more computation time. These are implemented by using Xilinx ISE design suite 14.7 and performed in Spartan 3 FPGA.

In Wallace tree [24] multiplier is designed by using binary to excess 1 converter and carry select adder. These techniques are used to minimize number of logic gates and partial product stages. But the Wallace tree with carry select adder is better and loss memory bottleneck, amount of LUT, when compare to Wallace tree with binary to excess 1 converter. In canonic signed digit [25] it is a comparison of binary number to CSD and new CSD recoding. By using booth technique, the new CSD recoding is better. When compared with binary to CSD, because its reduce power, computation time, area, delay, produce high speed and minimized overall hardware implementation and its more efficient. In multiplier architecture [26] the partial product generation by using 4:2 and 5:2 compressor and then finally the partial product accumulates by using

baugh-wooley multiplier to least the amount of partial product and electronic transistor count. But its increase amount of slices and computation time. These are implemented by using Xilinx tools, Figure 6 shows the. 8 bit baugh wooley multiplier.

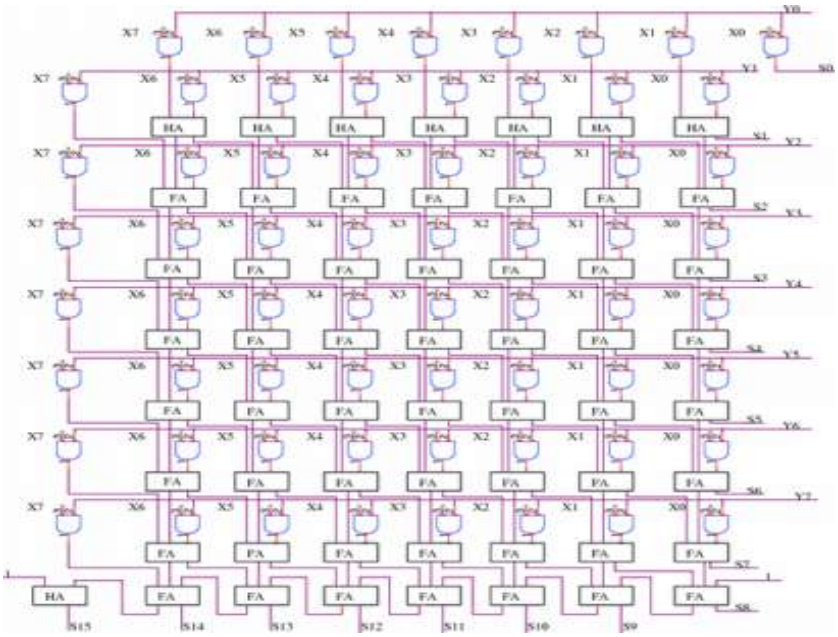

Figure 6. 8 bit baugh wooley multiplier

III. DIFFERENT MULTIPLIER ADDER AND APPLICATION

In Recent technology, the explosive growth of VLSI system and devices, the ability reduction of computer circuit has become unresolved downside. In application like communication system, telephone, transportable storage devices, low power dissipation and longer battery time period ought to be additional vital and respectable. To realize a protracted life operation of the device or circuit have quicker operation and low power consumption. Booth encoder [27] base on the radix 2^3 and 2^2 multiplier compared with (2^{n-1},2^n, 2^{n+1}) based RNS multiplier to reduce computation time and delay. These are implemented by using synopsis design compiler The figure 7 in 4 bit carry look ahead adder.

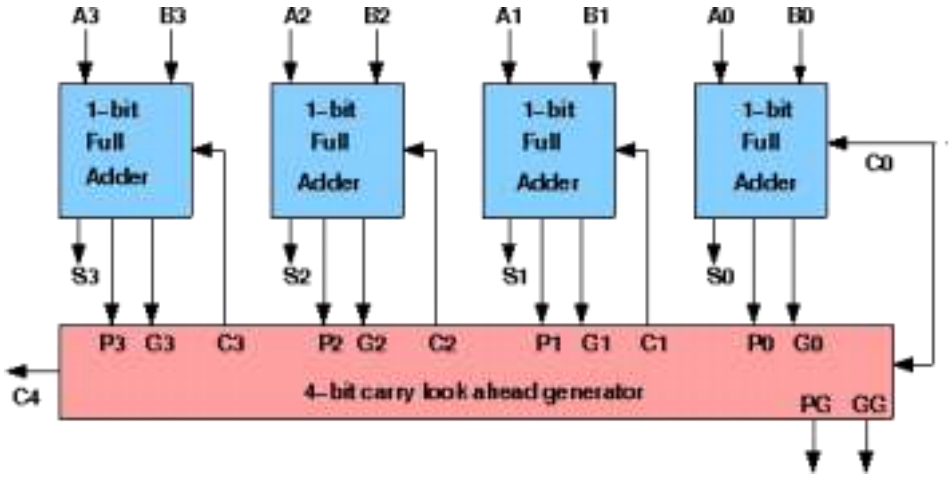

Figure 7. 4 bit carry look ahead adder

In Approximate Wallace tree structure [28] the partial product generating using booth bit pair recorder and partial product accumulates by using approximate Wallace tree structure with 4:2 compressor to minimize the amount of transistor count and maximize speed. These are enforced at gate level by exploitation Verilog high-density lipoprotein, then it's synthesized by Synopsys style complier exploitation 45nm open cell library. In modified Wallace tree structure [29] is applied with reduced complexity algorithm and modified adder is

used. This adder are designed by using low pass transistor logic based 2:1 multiplexers to reduce number of transistor, area, and switching short circuit power. The circuits are designed using 90nm technology and simulated in cadence virtuoso. In 4*4 multiplier [30] the partial product generation and accumulation by using comparison of array multiplier and canonical signed digit to reduce the size of area and increase speed. In both technique, the canonical signed digit is better when compared to array multiplier because the array multiplier having more delay and it's consume high power. These are implemented by using cadence virtuoso 90nm technology. In Wallace tree structure [31] the partial product generate both the full adder and hybrid CMOS design to improve the performance of the circuit, cut back the facility consumption of the circuit, the semiconductor count AND gate additionally reduced. These are implemented by using Tanner 45 nm. In radix 2 CSD multiplier [32] it is comparison of Horner CSD multiplier and pipeline CSD multiplier. Both techniques are used to reduce the partial product slices and delay. But the direct CSD is better than the Horner CSB multiplier. These are implemented by using Spartan 6 and vertex 7. In multiplier [33] the partial product generation by using array multiplier and Wallace tree structure with half adder, full adder, 1 bit full adder, and inverter circuits. By using theses technique, to reduced number of transistor count. But its produce delay and computation time. These are designed using cadence 180nm technology. The figure 8 in 4 bit rippler carry adder

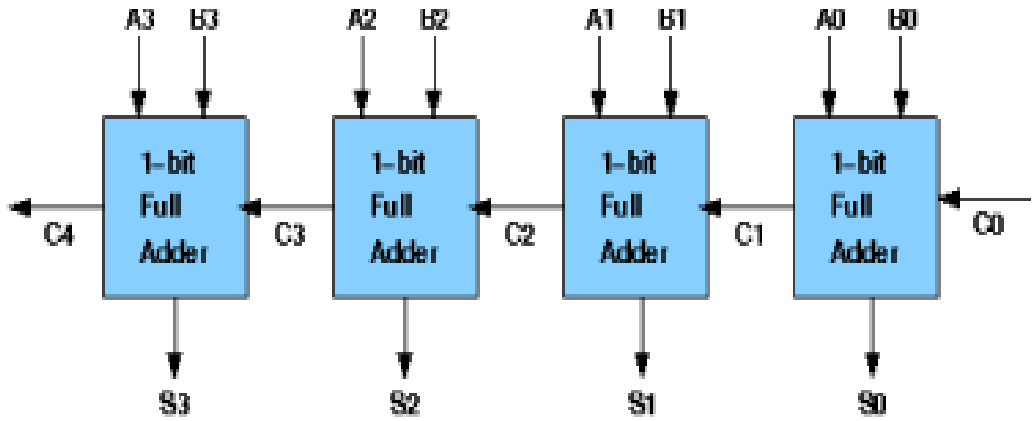

Figure 8. 4 bit rippler carry adder

In RSA processor [34] the multiplicand and multiplier are performed by using Urdha Tiryahbhayam and Nikhil am to reduce static power consumption, least area occupation, and less delay, and static power consumption. By using both, method, Urdha Tiryahbhayam is better in delay and device utilization compare with Nikhilam multiplier. These are implemented by using Xilinx Spartan 3 FPGA used for the development of security design in wireless detector network. In changed booth Wallace tree rule [35] one half is GDI primarily based booth encoder circuit and second half is partial product generation. By using this technique it's achieve low power, area, and delay. In multiplier architecture [36] the partial product generation by using booth recorder and canonical signed digit, accumulation by using carry look ahead adder to minimize the number of stages and increase speed when put next to alternative adder, carry look ahead adder is best, as a result of its increase speed, less power, delay, and area. These area units enforced by victimization Xilinx and synthesized victimization cadence tools. In four bit and eight bit Wallace tree structure [37] victimization 4-2 adder compressor device and 8-2 adder compressor device to cut back the quantity of stages and increase their speed. These 2 numbers, the eight bit Wallace tree number is best compared with four bit Wallace tree number. These are design synthesized using Xilinx ISE. In novel approximation for radix 4 booth multiplication [38] the partial product generated and accumulates to reduce the number of stages, increase speed, but its produce delay for high resolution. These are implemented in TSMC 65nm library using Synopsys design compiler. It is based on data aggregation [39] by using binary tree, folder tree with trunk phases and twing phases and wallace tree structure has three stages, first stages is partial product generation, second stages is reduction method by using 4:2 and 5:2 compressor, and then final stages are performed by using Sklansky adder ton ZED board can send the sink though WSN master development board to minimize small size, low cost and low power. In above technique the Wallace tree structure is better improvement in delay and area compare to binary and folder tree.

In approximate redundant binary multiplier factor [40] uses number eight booth encryption technique to attenuate the amount of partial product that may be summed victimization full adder, so circuit decrease complicated, delay, and low power consumption. In CSD algorithm [41] it is based on Vedic multiplier using

Canonical signed digit algorithm is performed image processing like edge detection. These techniques achieve high speed, less area occupation, but its needs more delay process because Vedic multiplier is complex and its need more computation time. These are implemented by using RTL schematic diagram of UT Vedic multiplier. The Figure 9 in 16 Bit Carry Select Adder

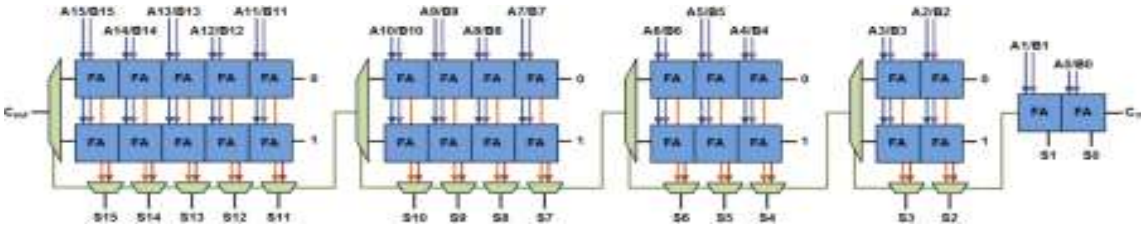

Figure 9. 16 Bit Carry Select Adder

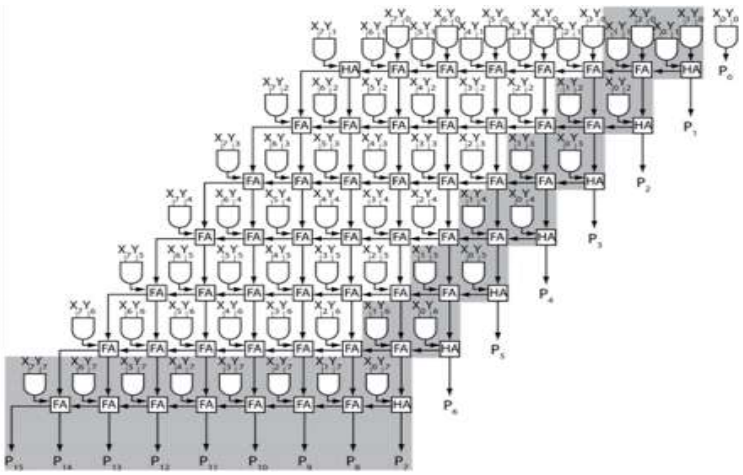

Figure 10. Bit Array Multiplier

In radix 16 booth multiplier [42] by using modified booth recoded, booth encoder, partial product generation, to minimize amount of slices and lesser area occupation. But its needs more switching activities are processing in this circuit. These are design using RTL. In Wallace tree approximate multiplier [43] has third stages, first stages are 15-4, second stage is 5-3 compressor and final stages are implemented by using kogge stone adder. Compressor are accustomed minimize delay and traditional adders mistreatment each half and full adder and it's avoid carry propagation. It's designed and simulated mistreatment Xilinx ISE fourteen- five software. In Wallace tree multiplier [44] it is based on three stages, 5-3, 15-4 compressor and final stages is kogge stone adder to fall depth number of partial product stages and maximize speed. But its needs more computation time to complete the process. These are implemented by using Xilinx ISE 14.7. In Wallace tree structure [45] it is comparison of Wallace tree with modified full adder and conventional Wallace tree structure with full adder used. To lesser the number of stages, slices, transistor gates. While comparing these two multiplier, the Wallace tree structure with modified full adder is better than the conventional Wallace tree structure. These are performed in Micro wind DSCH tool. The figure 10 Bit Array Multiplier

In 4 bit multiplier [46] it is consists of 2's complement generation, partial product generation, carry look ahead adder, then final stages are implemented by using Wallace tree structure with carry select adder, to minimize an area, computation time, but the carry select adder needs high usage of power is produced. These are implemented by using Micro wind tool and synthesized using DSCH. In Multiplier architecture [47] the reduction technique is changed to use carry choose adder is applied with binary to excess one convertor. Its increase speed, however binary to excess one convertor manufactures delay and high memory. These are design by using DSCH2 and Micro wind. In 32 bit Vedic multiplier [48] by using urdhva tiryahbhayam sutra are performance with both full adder and half adder to minimize a number of combinational delay, raised amount of slices. It is simulated on Xilinx ISE14.7. It is a comparison of [49] normal multiplier, dadda multiplier with 4:2 compressor and 4:2 double quantity blowers is used to minimize the delay, number of slices and precision. In both techniques the Wallace tree with 4:2 blowers is better to reduce, power, slices and memory when compared with normal dadda multiplier with 4:2 compressors. In parallel prefix adder with CMOS technique [50] it is an comparison of conventional Braun multiplier with ripple carry adder,

Braun multiplier using kogge stone adder, Braun multiplier using Brent-kung adder, and Braun multiplier by using modified Brent kung adder. By using these techniques, the Braun multiplier by using modified Brent Kung adder is less delay, reduce number of transistor when compared with conventional Braun multiplier is done by using tanner EDA tool in 250nm technology. The Figure 11 in 8 Bit Dadda Multiplier

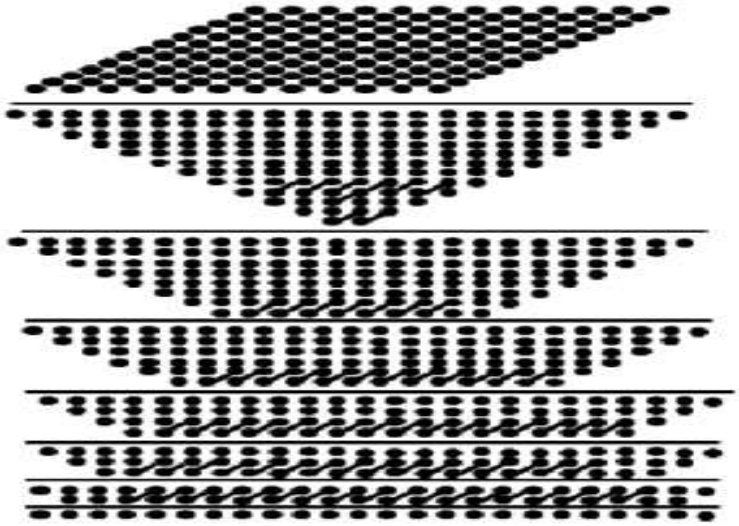

Figure 11. 8 Bit Dadda Multiplier

IV. COMPARISON OF VARIOUS MULTIPLIER

Reference	Multiplier	Delay (ns)	Power (µs)
	Urdhva tiryahbhayam	0.060	0.060
7	Nikhilam	12.838	26.39
15	4*4 Vedic multiplier	8.719	12.825
25	Binary to CSD.		
	New CSD recoding		
30	Array multiplier		
	CSD		
37	Wallace multiplier		
	with 4:2 adder		
	8 bit Wallace tree		
	multiplier		
	With 4:2 adder		
		7.89	5.60
		10.15	8.95
		13.97	8.797
		12.6917	7.828716
		3908.9	
		16.38	
		15.895	
		11.151	

40 Radix-8 booth technique 15.704 0.0029

V. CONCULSION

In this paper, overall review of different multiplier architecture and adder. The design approach is also applied with fixed and floating data type multiplier. This unit is very useful for all the real time application. All the multiplier are used to reduce the partial product and optimized their area, delay, power. In different technique, canonical signed digit and Wallace tree structure approach is addressed.

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