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Nano-Devices for High Speed Switching Applications: A Review

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Abstract- This paper details about research developments in nanometer scale for making integrated electronic devices. The nano circuits are majority used in digital circuits design, printed design boards, radio frequency (RF) signal processing, high quality precision sensors, etc. The efficient Metal Oxide Field Effect Transistor designs have very low power and are economical in fabrication. But as they are limited in I_{ON}/I_{OFF} Ratio, due to the need for faster switching devices at nanometer technology, new devices are developed. Among the various devices developed, Double-gate field-effect diode (DGFED) exhibit excellent features such as lesser short-channel effects, lesser OFF current (I_{OFF}) and greater ON current (I_{ON}). Double Gate FED (DGFED) suppresses the Short channel effects and significantly improves $_{ION}$/ I_{OFF} ratio. DGFED have lesser gate delay, larger Energy Delay Product (EDP), higher cutoff frequency and larger trans conductance.

Keywords: Double Gate Field Effect Diode (DGFED), I_{ON}/I_{OFF}, nano electronics, quantum dots, resonant tunneling, short-channel effects (SCEs), Tri-gate transistor.

I. INTRODUCTION

The shrinking of transistor with a length of less than 80 nm becomes more difficult and expensive to fabricate. This paper compares the alternatives with MOSFET's. The feature size of the silicon limited to half of the wavelength of the light due to diffraction in photolithographic processes. One more problem is not possible to dope silicon uniformly if the size of the silicon transistor is less than 50nm [1].

The silicon based design at micro scale level preferred in the electronic industry. Electronic devices using silicon reached to the extreme limits of miniaturization in size. The direction of research has been carried in two ways. One direction is fully depleted–substrate transistor (DST) and the tri-gate transistor with fully–depleted. Another direction is to change the silicon materials using Nano-materials with higher thermal, electrical and mechanical properties. The silicon can be replaced with carbon nano tube (CNT), Semiconducting Nano wire (S-NW), grapheme Nano ribbon (GNR), and molecular electronic devices [2]. By using nano-materials, the modified transistors reducing the size of electronic circuits [27].

The length of the MOSFET device is less than 80 nm [28], there is a problem caused by reducing gate oxide layer thickness to get high I_{ON}/I_{OFF} ratios [29]. Field effect diode (FED) [34] gives magnitude of the ON current is two times greater SOI-MOSFET.

II. STRUCTURAL DESIGN AND WORKING OF A MOSFET

The MOSFET is frequently used as a transistor in microelectronic digital circuits and Shockley's explain this device in 1952 [27]. The field effect transistor is three terminals device namely source, drain and the gate as shown in Figure 1(a). The electric field control the flow of current in MOSFET from the source to the drain is called a "field effect" transistor [3], For low gate voltage, few mobile negative charges developed between source and drain results in very small amount of current is flowing as shown in Figure. 1(b). When the voltage increases at the gate the channel has been created and more number of electrons flow to the drain from source results in dramatic rise in current as shown in Figure. 1(c).Due to small changes of voltage at the gate gives huge variations in the conductivity. MOSFET used as an applier [9].The process of reducing the size of the dimension of components with a constant factor is called "scaling."

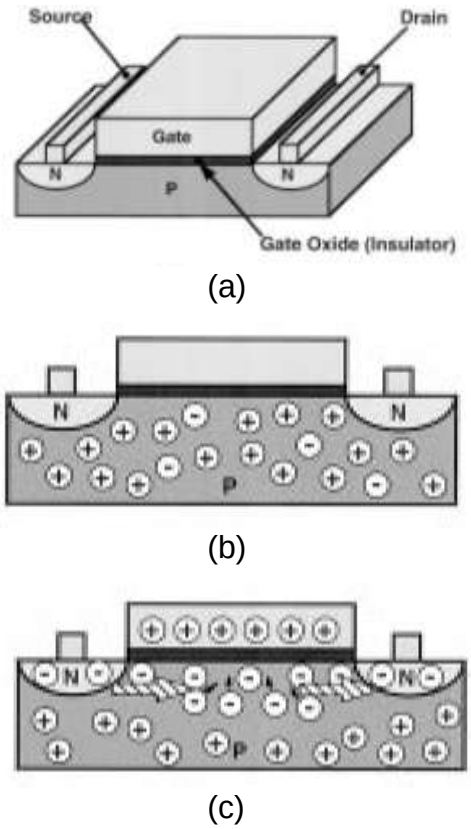


Figure 1. NMOS transistor. (a) Basic Structure. (b) V_{gs} = 0(c) Vgs> 0 [3]

A. Miniaturization of FET's

Transistors can be designed with a gate length less than 25 nm by using gallium arsenide [4], Because of biasing voltage over a short distance [5], large number of electrons comes out of semiconductor with high energies result in damage to devices[6]. This is one of the problems from the semiconductor in nano electronic devices. Heat dissipation occurs in the transistors cause to malfunction [7]. The operation of nano electronic devices mainly depends upon the electrons tunneling through barriers [8]. No uniform and Shrinkage of oxide layer under the gate avoid leakage of electrons between gate to drain.

III. SOLID-STATE QUANTUM-EFFECT AND SINGLE-ELECTRON NANOELECTRONIC DEVICES

A. Quantum Dot (QD)

A QD contains discrete number of electrons and can be treated as a metal or semiconductor well [10]. The quantity of electrons in quantum dot has been varied with electric field. If any two free electrons are occupy the same dot, because of their mutual repulsion those free electrons may occupy diagonal position in the quantum dot. The position of electron for logic 0and for logic 1 is shown in the Figure2.

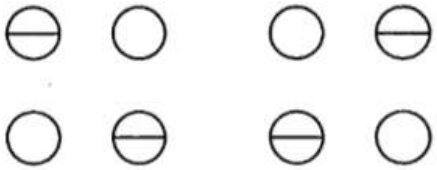


Figure 2. Logic values of Quantum Dots [1]

Logic design can be developed with quantum dots (QD). The significance of QDs is that a logic value cannot transmitted as conventional direction flow of current between two points in a wire, instead of that alignment the electrons using quantum alignment process to moving the logic value from one dot to next dot.

B. Resonant Tunneling Devices

The energy in the bands for source and drain can be adjusted to obtain variation in energy of quantum states and potential. The applied bias voltage is increased to lower the energy of all states.

In resonance or on state the bias potential applied will reduce the energy of unoccupied single electron quantum state in the specified range of energies of source conduction band inside the well [3].

The out of resonance or off state will block the current in the device. Hence the variable potential applied to change the tunneling current for on and off characteristics operation for the two terminal resonant-tunneling diode (RTD).An RTT device used as both switch and amplifier with adjusting the energy levels with respect to applied bias [4].

IV. ARCHITECTURE OF NANO DEVICE

Due to drastic scaling of transistors, the second order effects (SCEs) like off-state leakage current, drain-induced-barrier-lowering (DIBL) has been dominated. The technology trend proves that the limits on power dissipation beyond 10nm scaling are limited by off-state leakage current. Hence, there exists a need to lower off-state leakage current to as minimum as possible. In literature, several techniques are used to control it. They are by using fully-depleted silicon substrate, by choosing modified architectures such as double-gate FINFET and the fully-depleted tri-gate transistor, etc [2]. Figure.3 shows tri-gate devices which are connected in parallel that increases the total drive current.

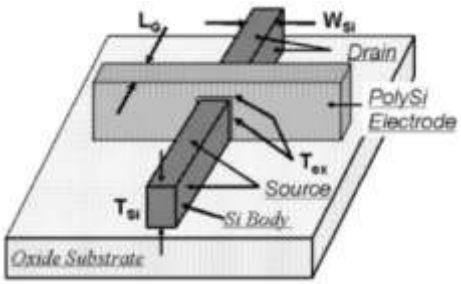


Figure 3. Tri-Gate Transistor Schematic [2]

Further the drive current can be improved by inserting number of silicon legs at the design area where the total drive current is the multiplication of the number of the legs, the drive current per leg as shown in the Figure.4. The other methods used are decrease in gate oxide layer below 0.8 nm but this gives rise to considerable leakage of gate voltage, which can be resolved by using high dielectric constant based gate oxide layer [2].

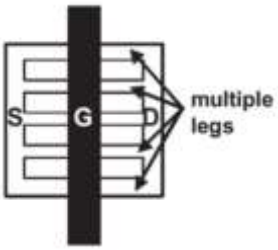


Figure 4. Top view of multiple Tri-gate legs [2]

V. FIELD EFFECT DIODE (FED)

The field effect transistor is modified into a Field Effect Diode (FED) [11] by splitting the channel into two regions under two gate electrodes separated by a distance for alternating electrons and holes accumulations to suit amplification and switching applications [12]. The source and drain doped with one type of impurity and channel region is intrinsic. When the positive voltage applied to GS and negative voltage applied to GD while drain to source voltage Vds. is positive [16], the FED should be forward biased. When the reveres voltage polarities are applied to GS and GD while keeping Vds is same then the FED should be reverse biased and becomes OFF as shown in the figure 5 (a). [32] The carrier densities in

the channel area is almost same and channel acts as intrinsic material when the FED in the OFF state. The structure of FED device is like n^+-i-p^+ instead of n^+-p-n-p^+ in the OFF state and the device still ON [33]. The drain and source parasitic resistances limit the current in FED.FED based digital circuits provide improvements in speed, area and power consumption compare with CMOS circuits [34].

This device has special features like being free from hot-electron effects (HCEs) and electrostatic discharge (ESD) [17]. Also in forward bias condition, due to exponential nature of diode action, the ON-state I_{DS} of FED will be much larger than that of MOS transistors [5]. Hence the main applications include in digital and analog circuits and systems, like the ESD protection [13], memory cells [14], high-speed digital logic gates [18], analog [19] circuits, etc.

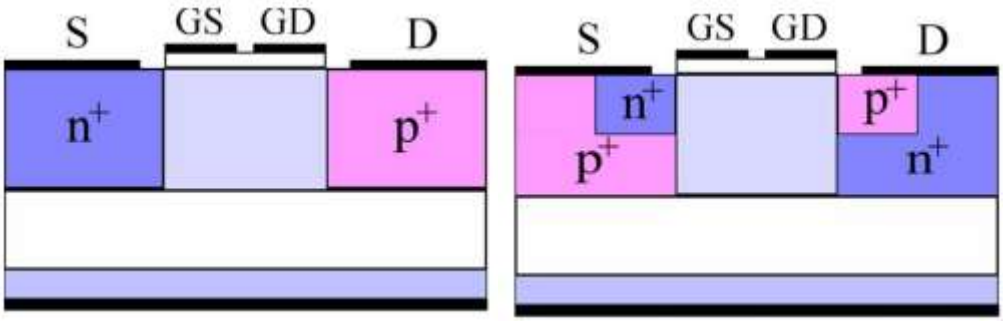
Still it has the drawback of increased in I_{OFF} due to increased gate bias for the length of the gate is less than 100-nm because of injection of additional minority carriers to channel to the drain from the source [15]. The other variations include the side-contacted FED (SFEDs), modified FED (MFED), heterostructure channel-based FED (H-FED), silicon on raised insulator (SORI) FED, grapheme-channel FED (GFED), double-gate FED (DGFED), etc.

MFED provide n^+-p-n-p^+ structure in the OFF state and device structure is shown in the figure 5(b).] [20]. A highly doped p and n new regions are placed inside the source and drain region called reservoirs which provide sufficient carrier densities under gates which reduces excess minority concentration of holes and electrons under GD and GS to maintain proper OFF state [21]. Due to more positive voltage applied to the drain compare with source, huge number of minority carrier injection takes place from drain to channel results in high majority carrier concentration and reduced OFF state current [36].

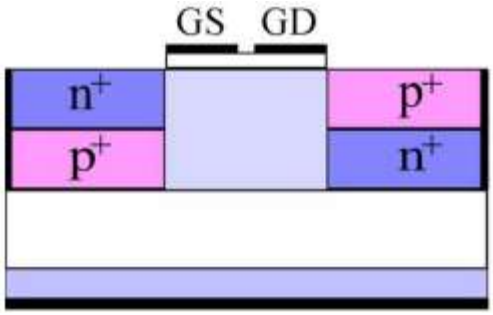
Author Neginet l., proposed Side contacted FED which is feasible to fabricate with trench technology. The Side contacts are developed to the drain and source by reactive ion etching as shown in the figure 5 (c) and which delivers high I_{ON}/ I_{OFF} ratio. But, the phenomenon of band-to-band tunneling increases I_{OFF} and limited scalability of MFED and SFED [24]. In SORI FED, oxide layer used in channel enhances the scalability below 20 nm which improves the gate control [25].

The H-FED is used to improve the gate delay and the I_{ON}/I_{OFF} ratio due to two separate Si/Ge regions at the center of the channel [22]. The GFED improves the I_{ON}/I_{OFF} ratio but has a drawback of early channel pinch of for very small V_{DS} [26]. Also it works as a MOSFET at large V_{DS} [26]. The DGFED decrease the Short Channel Effects (SCEs) ,increases I_{ON}/I_{OFF} ratio and performance [7].

In figure.6 (a) , the addition of p+ and n+ region at the source and drain respectively decrease the extra minority charges in the GS and GD, which reduces the I_{OFF} current in Side contact FED and Double Gate FED diodes[23]. The smaller whole concentration reduces the recombination rate but increases the resultant concentration of electron in the channel [30], thus high I_{ON} is achieved with lower power consumption in the DGFED with small turn-on voltage of V_{DS}. Also DGFED has smaller sub-threshold slope at small gate lengths should provide better scalability and better switching performance for digital applications. But at channel length below 40nm [31], the electrical properties exhibited by DGFED are suppressed due to opposite polarities of gate resulting in smaller net charge concentrations [5].

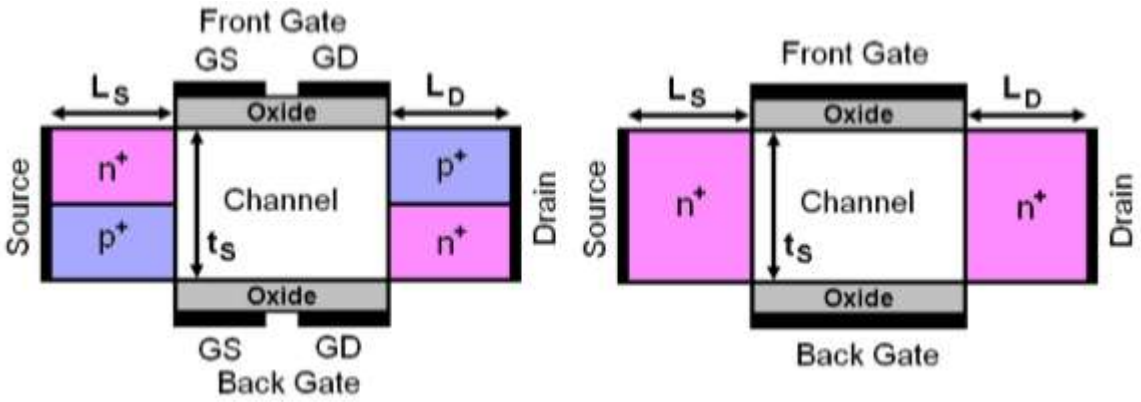


(a) (b)



(c)

Figure 5. Structure of (a) regular (b) M-FED (c) S- FED Structures



(a) (b)

Figure 6. Structure of (a) DGFED (b) DG MOSFET [5]

As V_{DS} increases, the electric field in the p-n junction increases, then the leakage current and I_{OFF} decreases in DGFED [35]. The Source and Drain Doping Concentrations are kept high which increases both I_{ON} and I_{OFF} of the DGFED. The gate oxide is thickened to reduce the concentration of electrons and concentration of holes during the ON-state in the channel. The t_{si} is decreased for highly doped channel regions which reduces the I_{ON}, but increases the gate delay time [26]. Also the gate is controlled over the channel which reduces IOFF considerably. DGFED does not enter into pinch off like DG MOSFET and current increases exponentially because of diode action. It provides higher ON current and smaller OFF current than DG MOSFET. DG MOSFET is shown in the figure 6(b).DGFED with lower I_{OFF}, higher I_{ON}, and larger I_{ON}/I_{OFF} ratio, use thinner oxide thickness, lower channel doping concentration, larger gate bias, smaller space between GS and GD, etc.

VI. Conclusion

The need for faster switching times enabled the need for higher I_{ON}/I_{OFF} ratio. Thus among the devices found in the literature, DGFED with proper device dimensions are suitable in high speed analog and digital applications as it suppresses the Short Channel Effects along with higher I_{ON}, lower I_{OFF}, higher I_{ON}/I_{OFF} ratio (especially for longer channels), small gate delay, smalls up threshold slope, large trans conductance, smaller EDP, and high cutoff frequency.

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