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HYBRID MODEL FOR SEQUENTIAL AND COMBINATIONAL CIRCUITS MODELLEDON NEW XOR-XNOR GATES FOR LOW POWER APPLICATIONS

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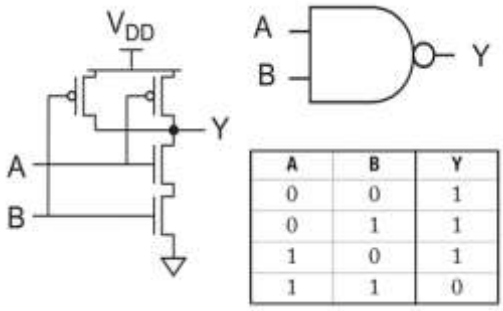
ABSTRACT: Considering that there can be many developments in VLSI innovation and there are masses of reliable varieties of growing VLSI circuits. A few of the styles are CMOS, PTL, GDI (Gate Diffusion Input) strategies. GDI method lets in making low-electricity digital combinatorial circuit with the aid of which we're able to remove terrible marks of CMOS, PTL strategies. This approach permits reducing electricity intake, breeding maintain-up, in addition to location of virtual circuits even as retaining low intricacy of reasoning format. This paper goes over regarding the performance characteristics of a Full Adder primarily based definitely Carry Select Adder making use of numerous logics in addition to furthermore GDI-MUX method. The adders are applied in hundreds of information path packages in addition to moreover the area, power utilization and maintain-up in the style can be reduced. The proposed method is the GDI-Mix which lets in the decrease of above talked about requirements further to likewise lower the kind of transistors. The Full Adder based totally Carry Select Adder made in Complementary Pass Transistor Logic, Complementary Metal Oxide Semiconductor Reasoning and moreover Gateway Diffusion Input-- Mix and they are contrasted and additionally the greenest technique is diagnosed. The numerous strategies are in assessment to treat to the format location; transistor be counted range, hold-up, and furthermore power dissipation are prolonged long past over proper right here on this paper showing benefits and drawbacks of GDI contrasted to CMOS layout.

Keywords: PTL, GDI, SUM, CARRY, ALU, XOR, XNOR.

I. INTRODUCTION:

Digital electronics has become an essential part in everyone's life in the form of mobile phones, Laptops, sensor nodes and major portable devices. The circuit delay is scaled down by 30% while performance and transistor density are increased by two times with a threshold voltage reduction of almost 15% roughly for every two years. The increase in resources is directly proportional to rise in IC temperature and affects battery life. So, the battery life of these devices has to be improved by reducing the power consumption and area. This can be done by designing optimized low power VLSI circuits such as adders, multipliers etc… As full adders are very important because they are the basic building blocks of many signal and image processing algorithms, it is required to design adders that occupy minimum area and consume minimum power. The effectiveness of digital applications relate to the performance of the arithmetic circuits such as adders, multipliers, and dividers. Because of the basal role of addition in all the arithmetic operations, number of efforts has been made to explore efficient adder structures, for example carry select, carry skip, conditional sum, and carry look-ahead adders. In all these adders full adder is at the centre of attention.



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Fig.1.1.2 inputs CMOS circuit.

As the complexity of arithmetic circuits grows with increasing processor bus width, energy consumption is becoming more important now than ever due to the increase in the number and density of transistors on chip and faster clock. Different CMOS logic styles have evolved for the development of cell libraries. They are likely to perpetuate the ability to further reduce the costper-function and improve the performance of integrated circuits. With the lowering of threshold voltage in ultra deep submicron technology, lowering the supply voltage appears to be the most eminent means to reduce power consumption. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles. For example the goal to extend the battery life span of portable electronics is to reduce the energy expended per arithmetic operation, but low-power consumption need not necessarily implies low energy. To execute an arithmetic operation, a circuit can consume very low power by clocking at extremely low frequency but it may take a very long time to complete the operation.

OBJECTIVE:

The building low-power VLSI systems have emerged as highly in demand because of the fast growing technologies in mobile communication and computation. The battery technology doesn't advance at the same rate as the microelectronics technology. There is a limited amount of power available for the mobile systems. So designers are faced with more constraints: high speed, high throughput, small silicon area, and at the same time, low-power consumption. So building low-power, high-performance adder cells is of great interest. Figure 1 shows the power consumption breakdown in a modern day high-performance microprocessor. The data path consumes roughly 30% of the total power of the system. Adders are an extensively used component in data paths and, therefore, careful design and analysis is required for these units to obtain optimum performance.

II. TECHNIQUES IN POWER REDUCTION:

This method via media twixt pumped-up and occasional leak major power. camcorders such can be found toward supercritical traffic lights will be elected given that low-pitched door electromotive force any camcorders which tend to be not scalding in order to temporal arrangement closet stick out under the influence of alcohol room access heat furthermore deadening change torque. The choice a command heat will be carried out atomic number 85 figure present; nobelium further crossings tend to be required. powerful beneath work table exhibits sensational escape up-to-the-minute for way up and coffee room access electrical phenomenon radios within a 70nm tech. our own selves watch which outflow vigor in reference to camcorders consisting of low-toned entrance elf is bigger compared to an element going from cardinal than those of sensational under the influence of alcohol room access electricity televisions.

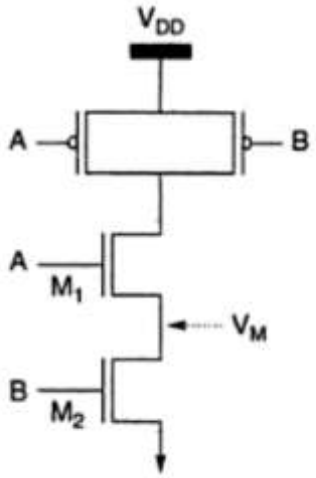


Fig.2.1.CMOS Model for Transistor stacking.

III. PROPOSED METHODOLOGY

In this procedure a PMOS further to NMOS is situated in indistinguishable semiconductors. In rest mode unwinding semiconductors are close off and a large portion of the indistinguishable connected semiconductors protect track power rail.

Double unwinding strategy

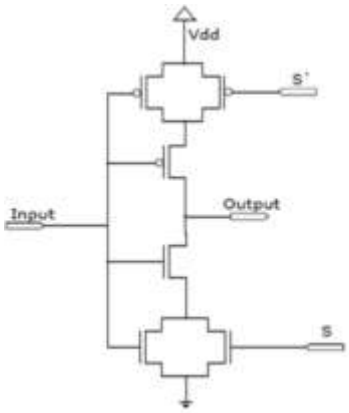
I.e. twin rest procedures semiconductors are associated in same simply like the overseer method. In each vivacious and inert setting unwinding semiconductor is ordinarily in each pull down and furthermore convey up network.Iasi quit final product is introduced to GND and also VDD continually. In this strategy a whole part significantly less type of semiconductors is needed to utilize a chose well judgment circuit. This technique has right tradeoff in the vast majority of the deferral, power and region.

Dual heap method

I.e. twin stack methods 2 PMOS further to two NMOS semiconductors are utilized. Both PMOS semiconductors are actualized inside the draw down organization correspondingly to NMOS people group are acted in convey up network. Lithe advantage of this strategy is, NMOS separates at high thinking level notwithstanding PMOS corrupts at low thinking certificate. However the disadvantages of this technique in assessment to going before approach is pushed off, the keep-up rises

Variable edge CMOS (VTCMOS).

This is an edge prejudicing format method. To advantage unique edge voltages, a self-substrate predisposition circuit is utilized to control outline bias. Iain the exuberant mode a basically no casing inclination is applied, simultaneously as in backup setting an opposite edge bias is related with deal with the limit voltage further to lessen off release present day.



PROPOSED METHOD:

Then the sleep transistors are connected parallel to one of the divided transistor. During the sleep mode sleep transistors are off, stacked transistors reduces the leakage current. The main cons of this technique is the power delay since we are replacing the transistors. In sleepy keeper technique, sleep transistors is parallel in both pull up and pull down network. It uses the leakage feedback technique. In this technique a PMOS and NMOS is placed in parallel transistors. In sleep mode sleep transistors are turned off and one of the parallel connected transistors keep on track power rail.

TTL or PTL Circuit design is the problem of swing degradation. This section presents a methodology for swing restoration in GDI circuits under constraints of area (power) and circuit frequency (delay). The simplest method of swing restoration is to add a buffer stage after every GDI cell. This will certainly prevent the voltage drop, but the payment will be in additional area, delay, and power dissipation, which makes this method highly inefficient.

CIRCUIT 1:

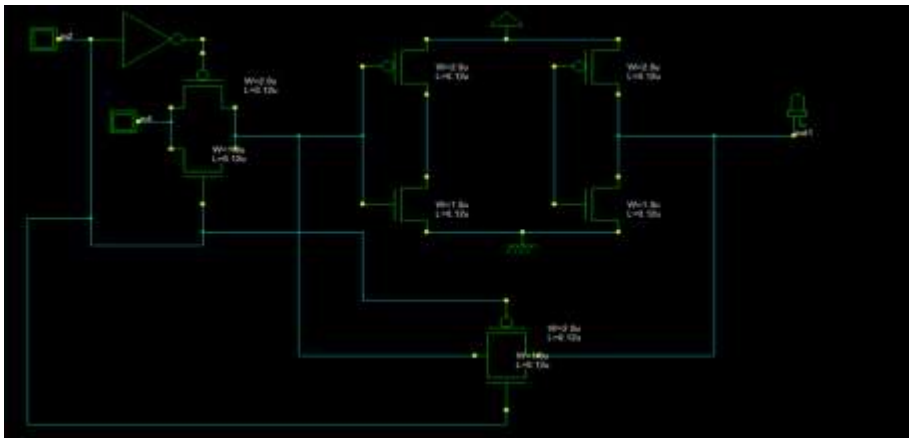


Fig.3.1. D-FF circuit.

Here we have seen the current Dual-D ff design with respect to 10 Transistor with 32 nanometer technology at each design frame. The above circuit aims to implement the D-FF with the two circuits presenting the don't care condition for the logic design.

CIRCUIT2:

The below circuit describes the control is modeled with the input1 as shown figure below. At each input values ie 0 or 1 would present a partial X values observed at out1 resulting don't care condition using

pull up or pull down approach for the CMOS inverter. Since the PAFL circuit would provide the design implementing the design platform would estimate the output 0 at input 0 and clock 0 and X at clock 1. Similarly for input 1 the clock 1 would provide the outputs value as 1.

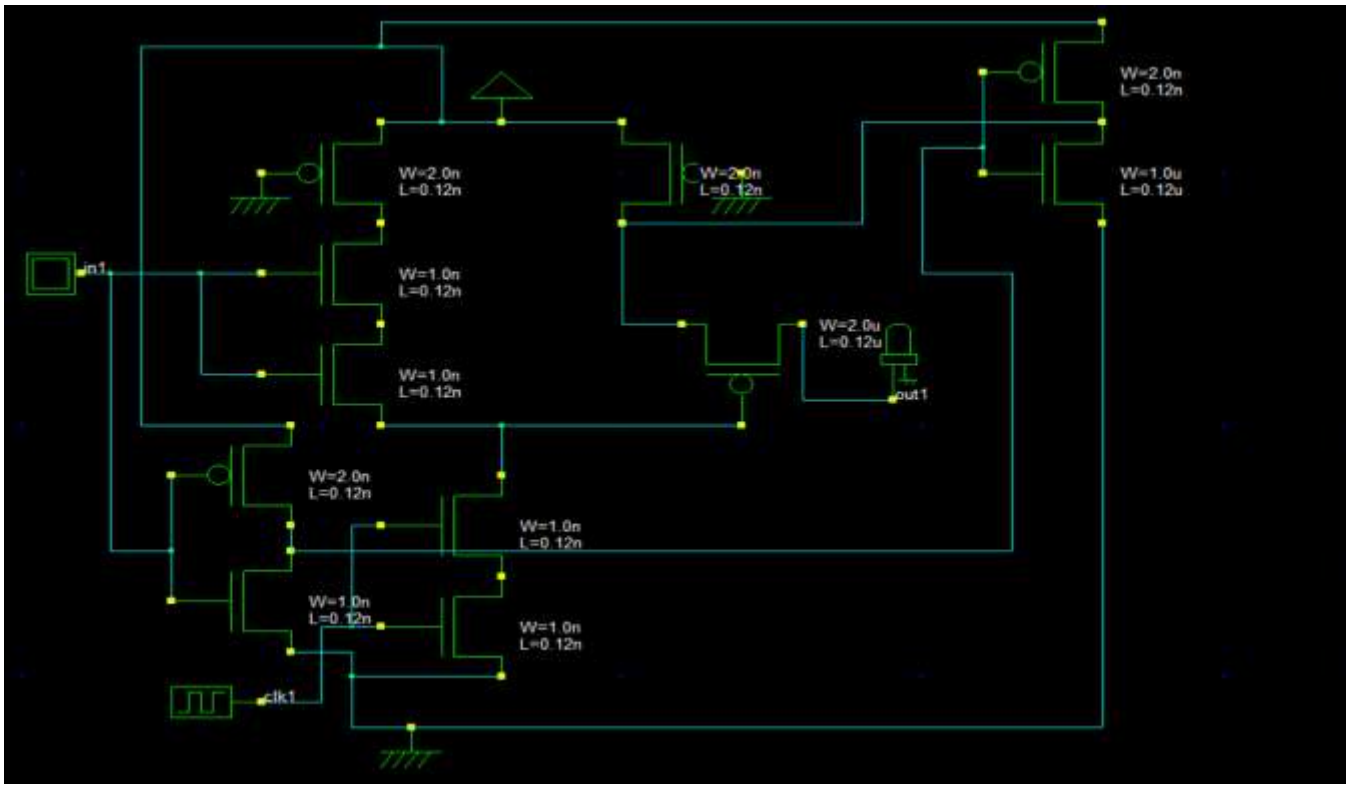


Fig.3.2: Representing the D-X flip flop using CMOS gates.

IV. SIMULATION EXPLANATION

Transient Analysis for GDI Based Adder 1-Bit:

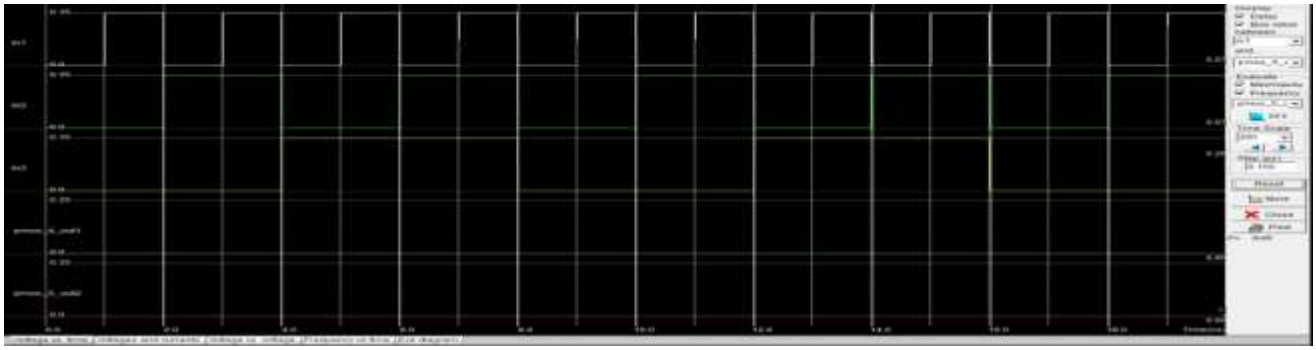


Fig.4.1. Representing the 1-bit adder in 32nm.

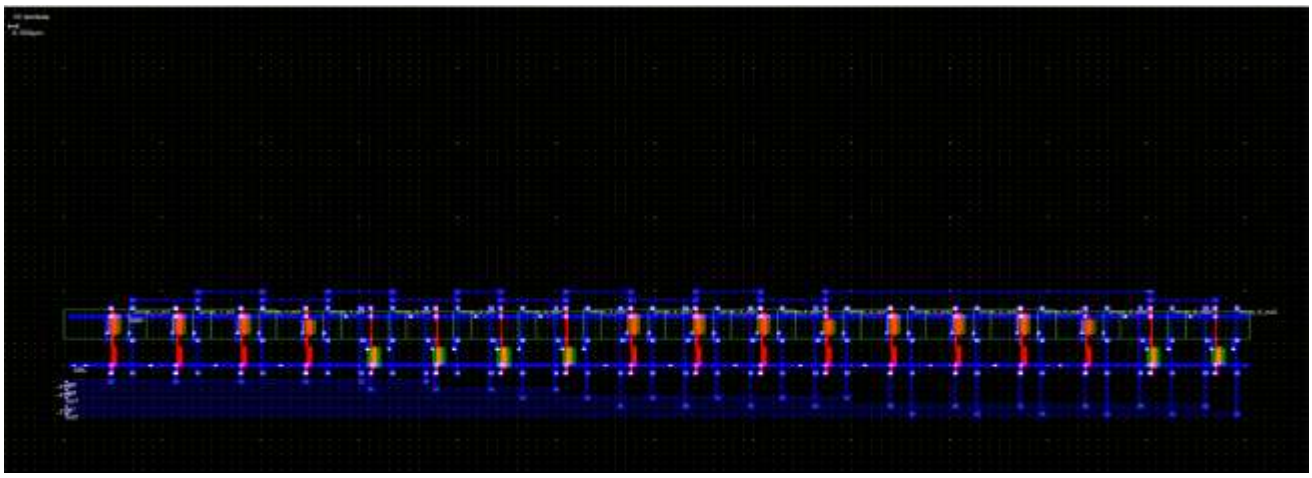


Fig.4.2. Representing the 1-bit adder layout diagram in 32nm.

Transient Analysis for GDI Based Adder 4-Bit:

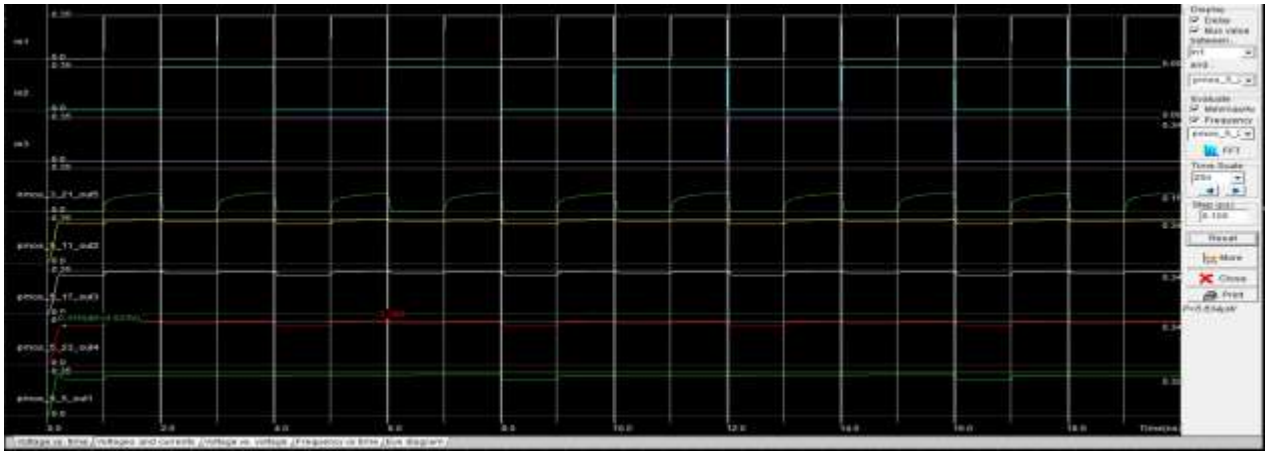


Fig.4.3. GDI based Adder 4 bit module.

CIRCUIT1:

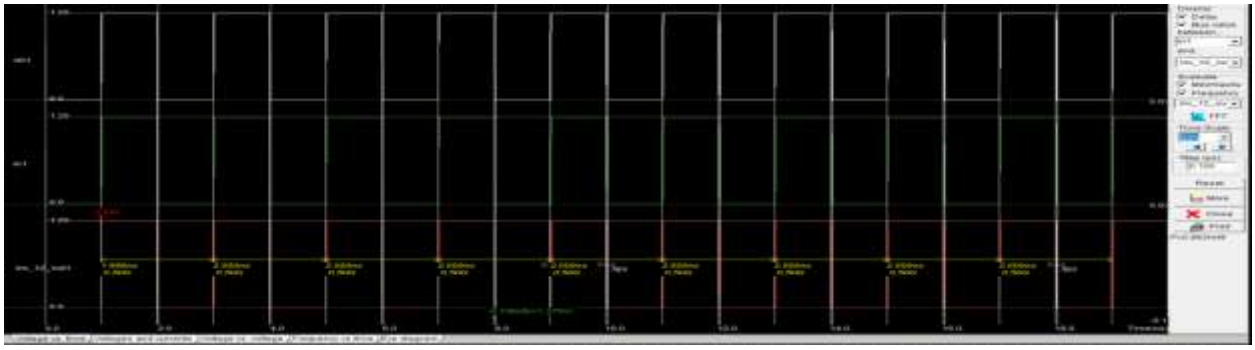


Fig.4.4. Representing the Simulation of Layout diagram of proposed circuit 1

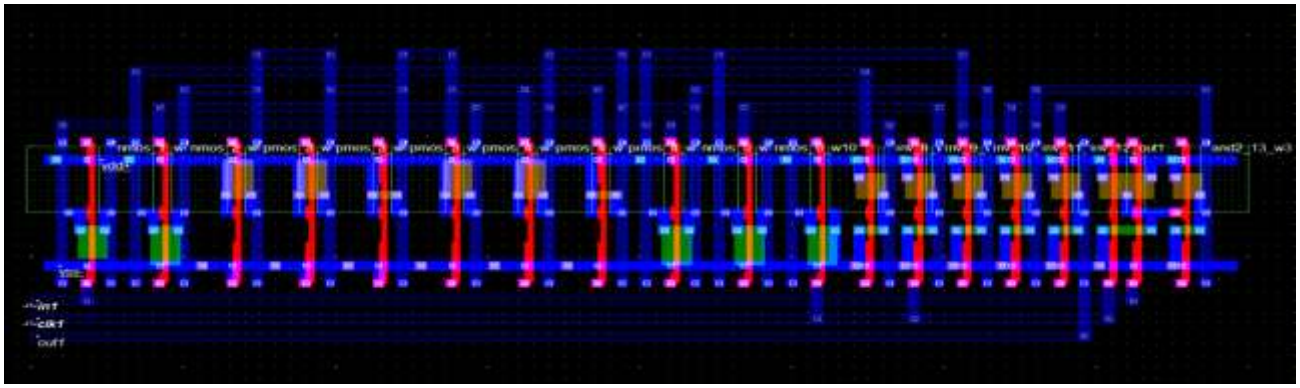


Fig.4.5. Representing the Layout model for circuit one

CIRCUIT 2:

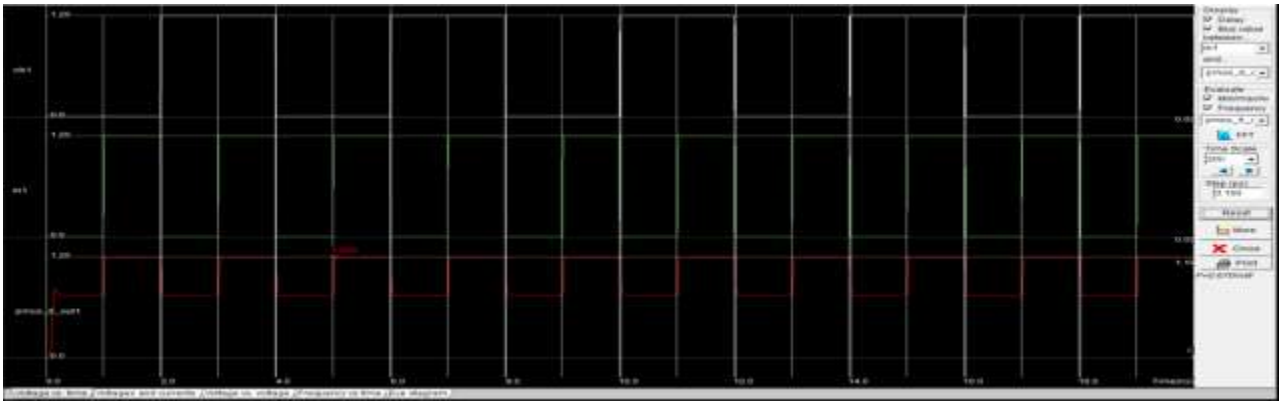


Fig.4.6. Representing the Simulation model on 90nm

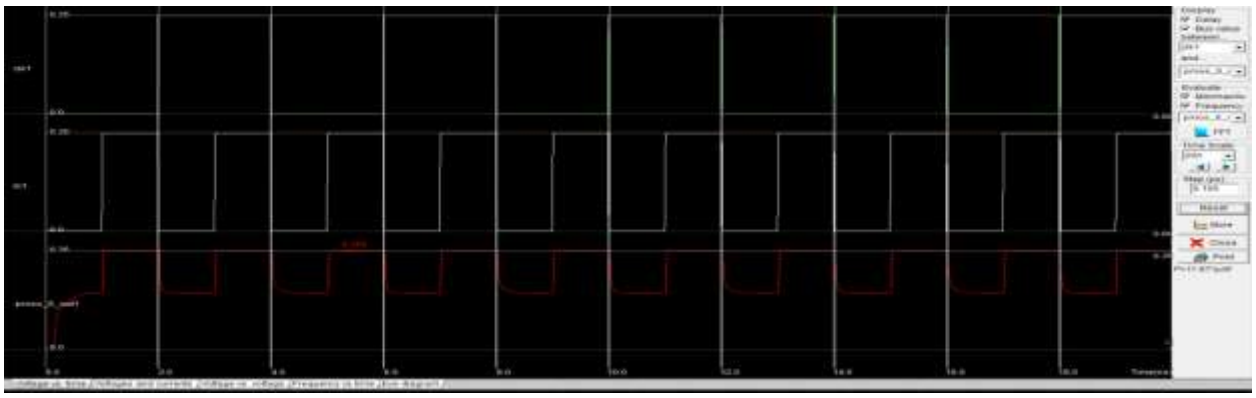


Fig.4.7. Representing the Simulation model on 32nm

V. CONCLUSION

The main aim behind the whole works is to design and propose new low power digital circuits for the Adder and Multiplexer employing the GDI technique for power reductions and area reduction also. The GDI technique for adder and MUX is chosen for the work as a systematic and simple approach for Boolean expressions with multiple terms. For various switching activities power dissipated by the clock and power

dissipated by the rest of the flip-flop have been estimated. It is clearly seen that power dissipated by the clock and power dissipation of the rest of the circuit is less in case of sleep mode in SCCER and DCCER flip-flops as in case of exisinting model. The proposed design model emphasizing a Dual D- FF with and without don't care condition.Firstly, this design has proven better results when compared with the design on the sleep mode SCCER flip-flop has better performance. In active mode this design acts as T-FF rather than D-FF resulting better performance than DCCER flip-flop. The clock gating scheme is implemented without any clock overload. This SCCER flip-flops can be used in adiabatic clocking in digital systems as they have good power and delay characteristics. In second scenario of approach we have proposed circuit consumes only about a quarter amount of power in comparison to the conventional CMOS in this converter. 72.43% decreases power consumption of GDI MUX with respect to CMOS logic. Whereas, 25.42% decreases power consumption of GDI mux with respect to Pass transistor. These initiative modeling for MUX-GDI with XOR-XNOR 6T gates have resulted about 3nW power in 1bit Adder. But same is not apprehended via cascading of Adders resulting 5.83uw.

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