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LOW POWER DIGITAL COMPARATOR MODELLING AND IMPLEMENTING FOR DSP APPLICATIONS

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ABSTRACT: Comparators are a basic design module and element in modern digital VLSI design, digital signal processors and data processing application-specific integrated circuits. This paper comprises of design of three different comparators for 2, 4 and 8 bit magnitude comparison. The above said designs are prepared using two different design approaches: Weighted Logic and PTL .The above two design approaches are designed in a way to endow with good quality performance. The performance of these three different comparators in the two design styles has been compared in terms of area and power consumption which are the important parameters that are considered while designing any digital circuit. The schematic are designed and simulated for its behavior using DSCH-3.1.The layout of simulated circuits are created using Verilog based net list file which is then simulated in Microwind 3.1 to analyze the performance of comparators for the two design styles at 45nm and 32 nm CMOS technology.

Keywords:PTL, comparator, IC, Adder, A/D converter.

I. INTRODUCTION:

Comparators are widely used in electronic circuits after operational amplifiers. They are also mostly popular as 1-bit analog-to digital converters. Analog to digital conversion efficiency mainly depends on the input sampling process. Comparator determines the digital equivalence of the analog signal with the help of its sampled input. In today's world, portable battery operating devices are growing rapidly due to the low power methodologies predominance in high speed applications. Power minimisation can be attained by inching towards feature size reduction techniques. The Short Circuit Channel (SCE) effect due to feature size reduction introduces various non-ideal ties and other process variations that affect the entire performance of the device. In analog-to-digital converters low noise margin, low power dissipation, low hysteresis, less offset voltage and high speed is essential for portable and mobile communication devices. The design of comparators with low power consumption, low offset along with the high speed forms the major interest in research today to achieve overall higher performance of ADCs. In the past, pipeline and flash based ADC architectures implement comparator based pre-amplifier designs. Offset voltage becomes a major constraint in preamplifier based comparators. Dynamic comparators are an alternative to overcome this problem to make a comparison during every clock cycle and need much low offset voltage. However, the power consumption is very high in dynamic comparators in comparison with the preamplifier based comparators. The major drawback of these dynamic comparators is the fluctuating output signal from the latch stage during clock transitions. This is due to the noise occurrence at the input terminals. The proposed converter design using multiplexer based full adder cell topology eliminates the noise at the input and reduces the power consumption and delay.

OBJECTIVE:

Corresponding steel-oxide-semiconductor (CMOS) is a era for building included circuits. CMOS innovation is made use of in microprocessors, microcontrollers, static RAM, and unique virtual correct judgment circuits. CMOS modern-day generation is likewise used for some of analog circuits such as photograph sensors (CMOS sensing unit), statistics converters, similarly to especially included transceivers for masses forms of interaction. Frank Wanlass patented CMOS in 1963 (US patent 3,356,858) whilst reaping rewards Fairchild Semiconductor.CMOS is also every so often referred to as complementary-symmetry steel-- oxide--semiconductor (COS-MOS).

The terms "complementary-symmetry" take a look at with the commonplace layout fashion with CMOS using complementary in addition to in share pairs of p-type in addition to n-kind metallic oxide semiconductor place effect transistors (MOSFETs) for reasoning talents.

2 vital features of CMOS devices are immoderate noise resistance and espresso static electricity utilization.Considering that one transistor of each is continuously off, the collection mixture draws extremely good electricity best for a brief time at some point of changing among on and stale states. Subsequently, CMOS gadgets do now not produce as plenty waste warmth as distinctive varieties of reasoning, for example transistor-- transistor reasoning (TTL) or N-kind metallic-oxide-semiconductor suitable judgment (NMOS) reasoning, which normally have a few fame gift furthermore while now not changing nation. CMOS likewise lets in a excessive thickness of reasoning competencies on a chip. It became within the most important because of this that CMOS have emerge as the most secondhand cutting-edge generation to be applied in very-large-scale integration (VLSI) chips.The word "metallic-- oxide-- semiconductor" is a reference to the bodily structure of particular state of affairs-impact transistors, having a metallic gateway electrode located on pinnacle of an oxide insulator, which in flip is on pinnacle of a semiconductor product. Aluminum become as quickly as utilized however now the product is polysilicon. Various fantastic steel gates have recovered with the advent of immoderate-κ dielectric products within the CMOS technique, as delivered with the aid of IBM and moreover Intel for the forty five nanometer node further to smaller sizes.

II. RELATED WORK &EXISTING METHODOLOGY

With the rapid increase in the use of portable electronic devices, the power dissipation has become a major constraint. As the technology grows rapidly and the device size scales down to the nanometer range, power dissipation, area and propagation delay are the major factors to be considered. The look for improving the performance of circuits based on CMOS logic resulted in the introduction of many logic styles like Pass Transistor logic, Transmission Gate logic, Double Pass Transistor logic and also many other hybrid logics. Pass Transistor logic is one of the most widely used logics for low power digital circuits. It has many advantages over CMOS, i.e. high speed, low power dissipation and lower interconnection effects. GDI Technique can overcome certain drawbacks of PTL Logic. A wide range of complex logic functions in which PTL was used, can be replaced by GDI Technique and this makes the circuit simple. Easier design of fast, low power circuits, with less number of transistors are enabled using GDI Technique. Arithmetic and logic operations are the inevitable part of all high speed and low power circuits in the field of microprocessors, digital signal processing, image processing etc. An Arithmetic Logic Unit with low power dissipation, lesser transistor count and lesser propagation delay can contribute much to the modern era.

EXISTING WORK:

Comparator is eminent to be a extremely basic and useful component of arithmetic units of the digital systems. In such systems, comparison of any two numbers is said to be an essential arithmetic operation that determine whether a number is greater than, equal to, or less than the other number. Subsequently, comparator is utilized for such operations. Magnitude comparator forms a combinational circuit to compare two numbers, let A and B, and lastly determine their comparative magnitudes and by this means relation between the two(equal to, less than, greater than). Fig depicts the fundamental block of N bit magnitude comparator. The result of comparison is represented by 3 binary variables that indicate whether A>B, A=B, or A<B. If two n-Bit numbers are to be compared then the circuit will have 2n inputs & 22n entries in the truth table. For 2-Bit numbers there shall be 4-inputs & 16-rows in the truth table, similarly, for 3-Bit numbers the truth table would comprise of 6-inputs & 64-rows.Figure 1 shows the block diagram of n-bit magnitude comparator.

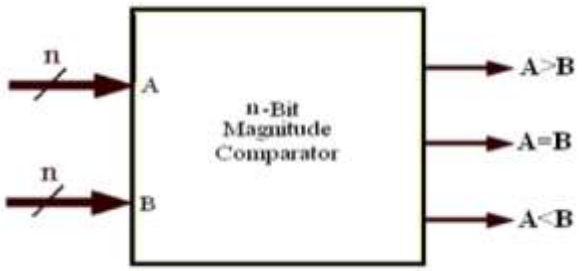


Fig.2.1.Model of 2 bit comparator.

In order to explain the functionality of this block, we look at 3 different cases (A>B, A<B and A=B). When the case is of unequal inputs, then the inequality output evaluates „1" and „0" in the cases of A<B and A>B, respectively, for correct functionality while the equality output is high. On the other hand, in case of equality A=B the equality output is low irrespective of the inequality output.

PTL logic

Chief edge of Pass Transistor Logic is to use purely NMOS Pass Transistors network for any logic operation. The fundamental variation of pass-transistor logic style and the CMOS logic style is that the source of the logic transistor networks is connected to some input signals instead of the power lines as shown in below Figure. In this design approach, transistor acts as a switch and thereby passes logic levels from input to the output.Such a design approach requires lesser number of transistors because one pass-transistor network (either NMOS or PMOS) is sufficient to perform any logic operation. Lesser number of transistors result in increased speed.

III. PROPOSED METHODOLOGY

Comparator is the fundamental building block in most of the analog to digital ADCs , they are used in memory sensing , decision..making. And control. Circuit like temperature protection and power control circuit 2010, oscillator, VLSI neural network etc. Comparator estimate the difference between two analog signals and respond accordingly in digital output. Comparator is used in computer system and device interface for equality. Comparator are used in many decoding circuitry like in computer and microprocessor also used in process controller and servo motor. The comparator can be as a one-bit analog-to-digital converter and it serves as the front-end circuit of most analog-to-digital converters. Many ADCs like high speed flash ADCs required high speed and low power consumption with small chip area. Low power operation is beneficial but when the supply voltage is reduced the transistor current also gets reduced which result in large time delay in the circuit. So designing the high speed comparator is a challenging task.

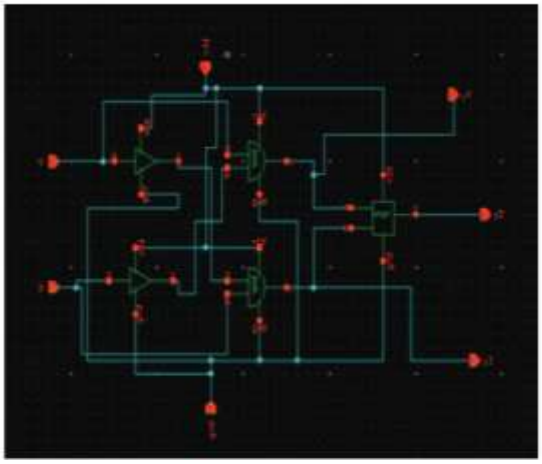
So designing the for low supply voltage need to have more transistor count to compensate the effect of low supply voltage, which again leads to more die area and power. A high speed synchronous comparator can be designed using differential input pair the challenge in comparator arises when the difference between the two analog circuit approaches zero, then a small disruption in the noise can affect the output of the circuit. So designing the comparator with the efficient gates that require less transistor, low power and area can make the system much efficient. Basic building gates used in comparator is XNOR gate. so designing the XNOR gate by applying different techniques can be make the system consume less power with better switching operation.

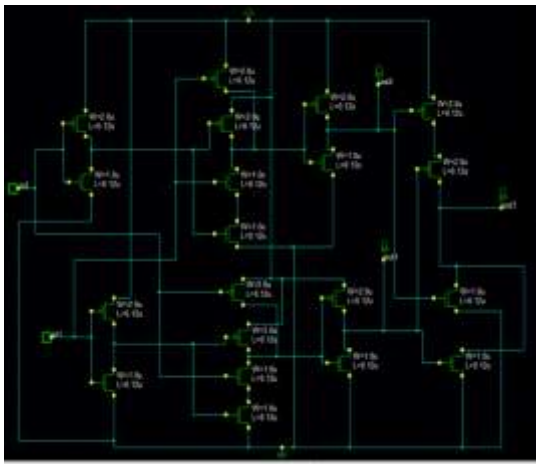
So CMOS technology is used to make gates as NMOS transistor passes strong logic 0 and weak logic 1 but PMOS transistor passes strong logic 1 and weak logic 0 [9]. So combination of these two can be used in a single switch that can drive its output at low or high voltage efficiently. There are many more technique to design it but the basic is to compare the two signal, write it truth table, find their equation and generate the output accordingly. In this paper we have designed 1 bit with 6T and 20 T comparator. By designing the 1 bit

comparator we get to know that XNOR gate is the basic one which will be used to design higher level of circuit. So we have also designed a 6T XNOR gate which reduces the transistor count by six.

CMOS DESIGN TECHNOLOGY FOR COMAPARATOR

Magnitude comparator is a circuit that compares two number X and Y and determine it relative output i.e X>Y, X=Y, X<Y .A. One bit comparator which compares the two input bits coming and gives output accordingly. Two input X and Y gives three output X>Y, X=Y, X<Y. The design model aim to represent the on bit design with 6T and 20T models for the current design methodology.





Here the EX-NOR gate used is made by using 12 transistor , and as a whole the circuit has 28 total transistor in it. The power parameter is 32 nano.

1) Another method of design it is to change the EX-NOR gate to XOR gate which reduce the transistor count from 12Tto 8T, and totally the transistor count became 30T with power 106 micro.

2) Another novel way of designing it is by using the subtraction logic , whose delay parameter is less as compare to other two ways . it's transistor count became 40T. with total power equal to 138.3micro. The logic defined is called so as it follow the basic rule of subtracting two signal. Which is explained as shown in figure. In this novel subtraction logic, we compare two number by subtracting them, as we know that in comparator there will three outputs one is a>b, a<b, a=b, by subtracting two numbers we derive our output in three different cases

In 2- bit comparator we used two full adders along with xors to subtract the given two numbers, after subtracting we arrive at three different cases as mentioned above, the further logic is designed to check where our output fits in the given above cases As we have seen in 2-bit comparator, in the same way for 4-bit comparator we used four full adders along with xor gates the given two 4-bit number, after subtracting the further logic is designed to check where our fits in the above mentioned cases If we want to design n-bit comparator, instead of going all the trouble designing k-map and using large number of gates, we can simply use 'n' full adders along with 'n' xors for the given two n-bit numbers and further logic to check whether the two numbers are less than or greater than or equal to each other. In this logic for A<B we can easily say that by connecting borrow node to output node. For A=B we connect an nor gate as it will only remain high when both the value of borrow and difference is same, and for A>B we connect an XNOR gate which will gives output high when difference is one and borrow is zero.

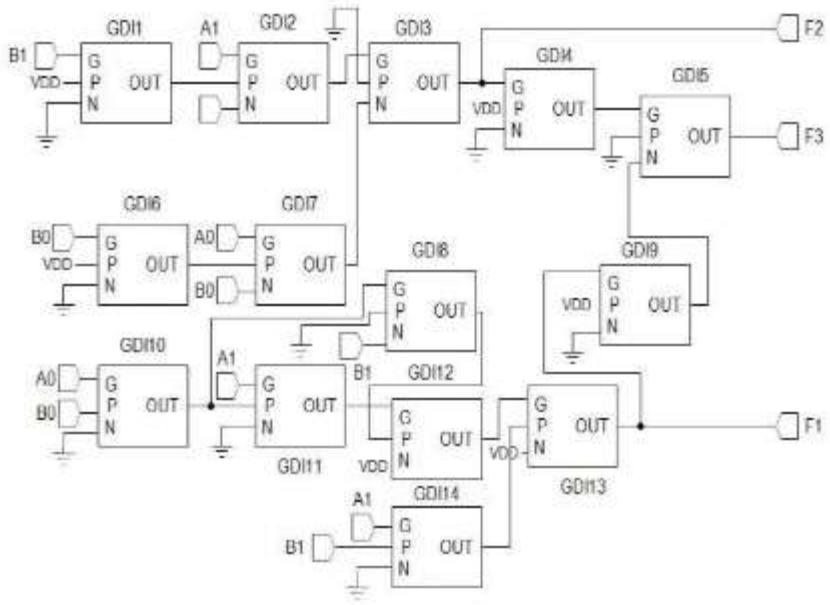


Fig.3.2. Proposed model.

IV. SIMULATION EXPLANATION

Power dissipation in a digital circuit can be mainly categorised into two components: One is dynamic dissipation that occurs due to the presence transient current during switching activity, discharging and charging of load capacitances and second is static dissipation that occurs due to the leakage current or other current continuously drawn from the power supply. The static power dissipation is the product of supply voltage and the leakage current. Power dissipation in the pass transistor logic is moderately high due to the presence of dynamic power dissipation in NMOS transistors. Power consumption mostly depends on the switching activity of the logic gates, which in turn depends on the inputs received on the comparator circuit. Power analysis can be estimated for a set of vectors by using a simulator and by evaluating the total capacitance switched during each clock transition at every transistor's node.

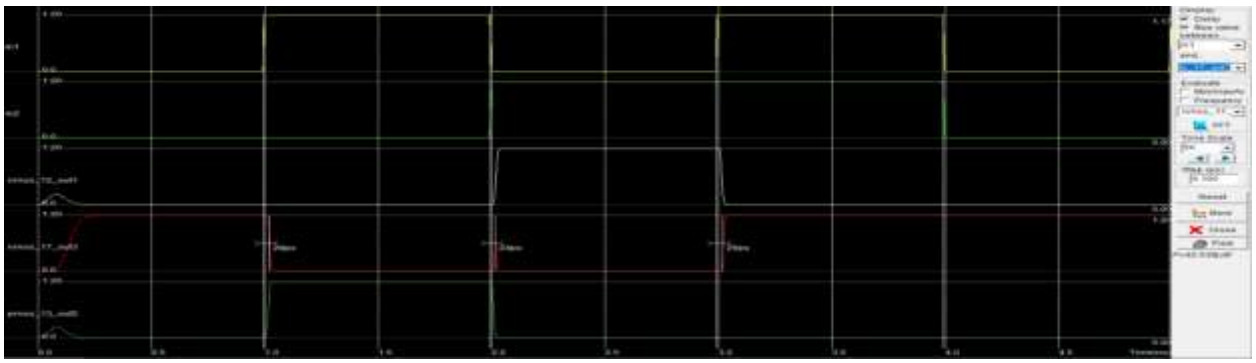


Fig.4.1. Simulation results.

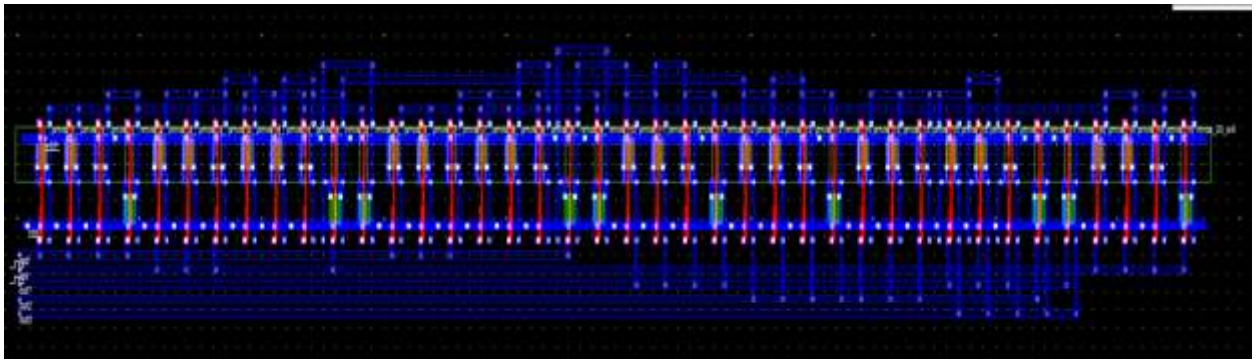


Fig.4.2. Output results.

V. CONCLUSION

We have presented different design of a comparator total two different types of designing the comparator is discussed with a novel architecture of a subtraction logic in it and we come to conclusion that a subtraction logic gives us good parameter of power delay product(PDP) as compare to all other design. Designing the comparator having a 6T XNOR gate gives us less delay as comparing to simple design. The design is been tested in 1.8 voltage supply and all other parameter is been discussed.

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