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Design and Analysis of 1.2KW Interleaved Synchronous Buck Converter Design for Aviation Systems

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Abstract:- The main goal of this work is to create a battery-powered 1.2kW interleaved synchronous buck converter for aviation systems with lower losses than current topologies. It is hoped to reach a loss reduction of at least 5%.Military planes like the F-22 and commercial planes like the Boeing 787 use 270V DC for their battery systems. While the 270V DC system has some advantages, such as reducing losses and the size of passive elements, old avionics that have been developed, manufactured, and used since World War II have some limitations. It's possible that it won't work with the 270V DC system. For both old and new systems, converting from 270V to 28V appears to be very promising. As a result, this study proposes a buck converter design for 270 to 28V conversion to adapt older avionics technology to contain innovative achievements. The study of an interleaved synchronous buck converter based on SiC MOSFETs with a double loop PI controller is provided. The paper explains the design principles and speculates on possible innovations. Simulations are used to validate the definition.

Keywords: DC Sysem,PI controller, open loop,closed loop, Mosfet, feedback, PID controller.

I. INTRODUCTION

Pneumatic and hydraulic applications have largely been replaced by electrical equivalents in recent aircraft innovations [1-2]. The 270V DC system, which has recently been used in aircraft, has a number of advantages. Loss reduction in transmission and energy storage element sizing, for example. Using 270V DC, it is simpler to supply the necessary power to the avionics with lower losses. It also makes supplying 115V AC to the machine with smaller and simpler inverters easier. The avionics that have been designed, manufactured, and used since WWII may not be companionable with the 270V DC system. To allow the use of those avionics, a buck converter can be utilized to adapt previous voltage levels and standards. Circuits for the same voltage spectrum but low power applications in general are available on the market [3-6]. This shows the need for a circuit design that can handle a lot of electricity.

In tele-communication power supplies, parallel dc–dc converters are commonly used. To regulate the bus voltage and allow load sharing, they use closed-loop feedback control [1]-[2]. These closed-loop converters are inherently nonlinear systems. The switching nonlinearity and the interaction amongst the converter modules are the two main sources of nonlinearities. However, in this field of power electronics, studies have largely relied on linearized averaged (small-signal) models [3]. Small-signal analyses cannot predict the basin of attraction of the nominal solution and the dynamics of the system after the nominal solution loses stability when a nonlinear converter has solutions other than the nominal one [14]. Furthermore, small-signal models are incapable of predicting the dynamics of a switching converter in a saturated state. Clearly, linear controllers [3] built for such systems are not always capable of providing reliable solutions and optimal efficiency.

Studying the dynamics of a parallel-converter system using bifurcation analysis is one way to get the best results out of it. In this process, the system's stable and unstable dynamics are investigated as a parameter is modified. Nonlinear maps [2] are used since almost all converters are nonlinear and nonautonomous. The bifurcations are defined as static or dynamic depending on the movement of the Floquet multipliers associated with these charts. The benefit of this method is that it allows the converter's output to be optimised if the dynamics of the structures outside the linear area are established. [8] discusses how to

put this strategy into action. Another solution, which is the subject of this discussion, is to design a robust nonlinear controller that achieves global or semi-global stability of the nominal orbit in the parallel converter's operating region [5]–[7].

Many studies of nonlinear control of standalone dc–dc converters [7] have recently been published, with particular emphasis on variable-structure controllers (VSC) [9], Lyapunov-based controllers, feedback linearized and nonlinear controllers [5]–[7], and fuzzy logic controllers [58]–[60]. However, aside from feed forward and feedback disturbances, there are few studies on the nonlinear control of parallel dc–dc converters, where, unlike standalone converters, there is a clear interaction among the converter modules. A fuzzy-logic compensator for master-slave control of a parallel dc–dc converter is proposed in [3]. The fuzzy inference rules are derived using a proportional-integral-derivative (PID) specialist, and the controller is more stable than linear controllers. The control architecture, on the other hand, is strictly heuristic, and the overall system's stability has yet to be proved.

A VSC for a buck converter using interleaving was built in [31]. The interleaving scheme, however, is limited to three parallel modules. Furthermore, this paper provides no information about the nature and stability of sliding manifolds. We suggest integral-variable-structure control (IVSC) schemes for parallel dc–dc buck converters in this paper. Since the control and plant are both discontinuous, a VSC is an obvious option for power converters. All of the nonlinear controllers listed earlier [7] that aren't based on VSC depend entirely on smooth averaged power converter models. As a result, the regulation can only be applied to a reduced-order manifold [8].

The IVSC has many of the characteristics of a VSC, such as design simplicity, dynamic response, and robustness. Furthermore, the IVSC's integral operation removes the bus-voltage error and the error between the load currents of the converter modules under steady-state conditions, and it reduces the effect of parasitic on the closed-loop mechanism due to very high-frequency dynamics. Finally, when the error trajectories are inside the boundary layer, we can reject mismatched disturbances and maintain the steady state switching frequency by adjusting the control using the principles of multiple-sliding-surface control (MSSC) or the block-control principle [13]. We use some important simulation results to back up our theoretical findings. We display how converter modules perform under steady-state and transient conditions, as well as when their parameters don't fit.

MODEL OF PARALLEL DC–DC BUCK CONVERTER

The dynamics of parallel buck converters (shown in Figure 1) are regulated by the following differential equations, assuming ideal switches: (1) where the input voltage is represented by the switching functions.

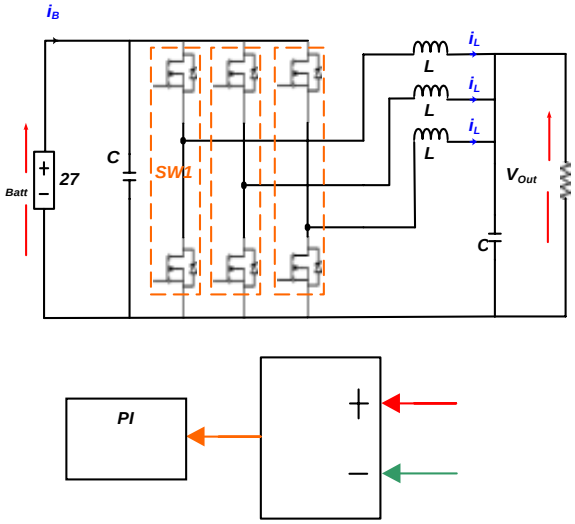


Figure. 1. The proposed interleaved synchronous buck converter

An interleaved synchronous buck converter topology for aircraft systems is proposed in this report. This topology and its control block diagram are shown in Figure 1.

II. THEORETICAL BACKGROUND

When designing for an aircraft application, the weight and scale of the power electronic elements can be very important. Interleaved systems result in fewer ripples at the circuit's input and output. As a result, they have smaller energy storage components than single buck converters, which have larger inductors or capacitors. They Due to switch fault tolerance, they also have higher reliability [7]. When each converter outputs the same current as the non-interleaved converter, the output current is N times higher. Due to the requirements for high current and low voltage performance, the proposed interleaved topology is suitable [7-9]. Furthermore, as opposed to a simple buck topology, synchronous converters have a number of advantages. Synchronous converters have a higher performance and are ideally optimised for high-frequency applications than non-synchronous converters with no forward voltage drop [10]. Different topologies exist, such as the dual active bridge topology [11]. To improve converter performance, this topology employs wide-bandgap SiC semiconductors. The use of GaN or SiC transistor switches in the converter system will result in significant loss reduction [12]. As a consequence, SiC MOSFETs are used in the built topology. MIL-STD-704 specifies the design specifications. Table 1 shows the DC system specifications for both 28V DC and 270V DC systems. The MIL-STD-704 [13] specification contains transient voltage limits.

Table 1. Voltage Standards[13]

	Limits	
	28 V DC System	270 V DC System
Steady State	22.0 To 29.0 Volts	250.0 To 280.0 Volts
Distortion Factor	0.035 Maximum	0.015 Maximum
Ripple Amplitude	1.5 Volts Maximum	6.0 Volts Maximum

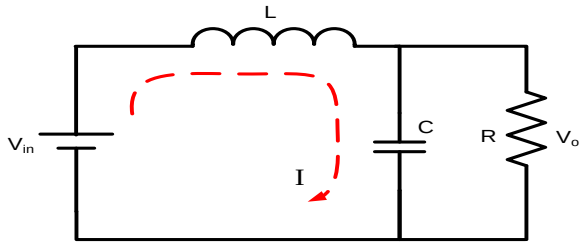
III. PROPOSED TOPOLOGY

Three interleaved buck converter stages are recommended by the report. For buck switching, both stages use two switches. A double loop feedback controller drives each switch couple (SW1, SW2, SW3). Each control signal collects current data from IL1, IL2, and IL3 and modulates SW1, SW2, and SW3 in turn. 100kHz switching frequency creates 300kHz ripples at the system's output waveforms while using the three-level interleaved point. Since this high-frequency ripple is simple to filter, a smaller output capacitor is needed. Furthermore, if the driving signals of N converters each have a 2/N phase shift, the converter's output filter may be reduced [13]. The explanation for this is that each drawback has been included. In addition, if a switch fails, the interleaved system's remaining two stages will continue to operate within the MIL-STD-704 DC voltage requirements [14].

Design of Converter

The source voltage is Vin, and the source current is Is. The key switch is S1, the diode is D, the inductor is L, and the capacitor is C. V0 is the output voltage, and R is the attached load.

When S1 is turned on and the diode is turned off.



$$V_{in} - V_0 = L\frac{dI}{dt}$$

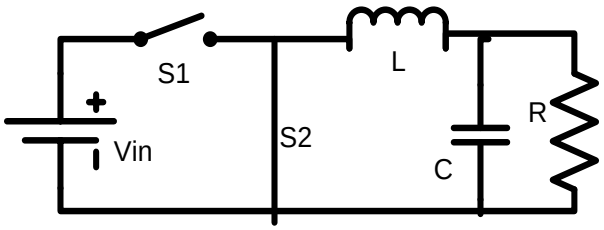
Assume $dI = I_2 - I_1$

$$dt = t_1$$

$$V_{in} - V_0 = L\frac{\Delta I}{t_1}$$

$t_1 = \frac{\Delta I \times L}{(V_{in} - V_0)}$ (1)

When switch is OFF and



$$-V_0 = -L\frac{\Delta I}{t_2}$$

$t_2 = \frac{L\Delta I}{V_0}$ (2)

Total switching period T

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I L V_{in}}{V_0(V_{in} - V_0)}$$

This simplifies to

$\Delta I = \frac{V_{in} D(1-D)}{f_L}$ (3)

The average capacitor current is

$$I_c = \frac{\Delta I}{4}$$

$$V_c = \frac{1}{C}\int i_c dt$$

Which gives $\Delta V_c = \frac{\Delta I}{8fc}$

Substitute ΔI

$\Delta V_c = \frac{V_{in} D(1-D)}{8LCf^2}$ (4)

V_{in}=320 V d.c , V_0=144 V

P_0=3.6 kW, I_0=25 A

f = 50Hz , D=0.5

Assume ΔI, ΔV_c as 5% & 2% ripples

The value of 'L' is calculated as I_0=I_L=25,

$\Delta I = \frac{5 \times 25}{100} = 1.25\ A$

$$L = \frac{320 \times 0.45 \times (1 - 0.45)}{50 \times 10^3 \times 1.25}$$

L=1.26mH

The Value of 'C' is calculated as $\Delta V_c = \frac{2\times144}{100} = 2.88\ V$

$$C = \frac{320 \times 0.45(1-0.45)}{8 \times 1.26 \times 10^{-3} \times 2.88 \times (50 \times 10^3)^2}$$

$C = \frac{79.2}{72576 \times 10^3} = 1.1\ \mu F$

The above analysis describes nothing about the devices ideality and its control circuit. The switching losses are to be considered while selecting or designing the circuit components and ratings.

IV. SMALL SIGNAL ANALYSIS OF BUCK CONVERTER

$$\begin{bmatrix} L\frac{di_l(t)}{dt} \\ c\frac{dV(t)}{dt} \end{bmatrix} = \begin{bmatrix} (-R) & 0 \\ 0 & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_l(t) \\ V(t) \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_g(t) \\ 0 \end{bmatrix}$$

$$\mathrm{Y} = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} i_l(t) \\ V(t) \end{bmatrix}$$

$$\begin{bmatrix} L\frac{di_l(t)}{dt} \\ C\frac{dV(t)}{dt} \end{bmatrix} = \begin{bmatrix} -R & -1 \\ 1 & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_l(t) \\ V(t) \end{bmatrix} + \begin{bmatrix} 1 & -1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_g(t) \\ 0 \end{bmatrix}$$

$$\mathrm{Y} = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} i_l(t) \\ V(t) \end{bmatrix}$$

$$\mathrm{A} = \mathrm{A1} * \mathrm{D} + \mathrm{A2} * D'$$

$$\mathrm{B} = \mathrm{B1} * \mathrm{D} + \mathrm{B2} * D'$$

$$\mathrm{C} = \mathrm{C1} * \mathrm{D} + \mathrm{C2} * D'$$

Where D' = (1-D)

$$\mathrm{A} = \begin{bmatrix} -(R) & -D' \\ D' & -\frac{1}{R} \end{bmatrix}; \mathrm{B} = \begin{bmatrix} 1 & -D' \\ 0 & 0 \end{bmatrix};\ \mathrm{C} = \begin{bmatrix} 1 & 0 \end{bmatrix}$$

$$\begin{bmatrix} L\frac{di_l(t)}{dt} \\ c\frac{dv(t)}{dt} \end{bmatrix} = \begin{bmatrix} (-R) & -D' \\ D' & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_l(t) \\ V(t) \end{bmatrix} + \begin{bmatrix} 1 & -D' \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_g(t) \\ 0 \end{bmatrix}$$

$$Y = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} i_l(t) \\ V(t) \end{bmatrix} \mathrm{y} = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} i_l(t) \\ V(t) \end{bmatrix}$$

$$\hat{X} = A\hat{x} + B\hat{u} + \{(A_1 - A_2)X + (B_1 - B_2)U\}\hat{d}$$

$$A_1 - A_2 = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$$

$$B_1 - B_2 = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}$$

Linearized to standard form

$$G_{v_d}(s) = G_{d_0}\frac{\left(1-\frac{s}{\omega_2}\right)}{\left[1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2\right]}$$

$$= \frac{V_0}{D'} \times \frac{\left[1-\left(\frac{S}{\frac{D'}{D}\cdot\frac{R}{L}}\right)\right]}{1+\left[\frac{S}{\left(D'R\sqrt{C/L}\right)\left(\frac{D'}{\sqrt{LC}}\right)}\right]+S^2\left[\frac{1}{D'/\sqrt{LC}}\right]}$$

Considering the values Vin=320V, R_L=0.2Ω, L=1.26mH, C=1.1µF, R_0=25Ω

V. SIMULATION

Figure 2 shows a simulation of an interleaved synchronous buck converter using PSIM simulation software. The switching losses are ignored in the simulation. To comply with MIL-STD-704 [14] requirements, circuit and simulation parameters are realistically chosen. The ripple levels and voltage tolerances meet the requirements. For element sizing and a single switch failure scenario, optimal working conditions are taken into account. The optimum working scenario with the PI controller is simulated in this article.

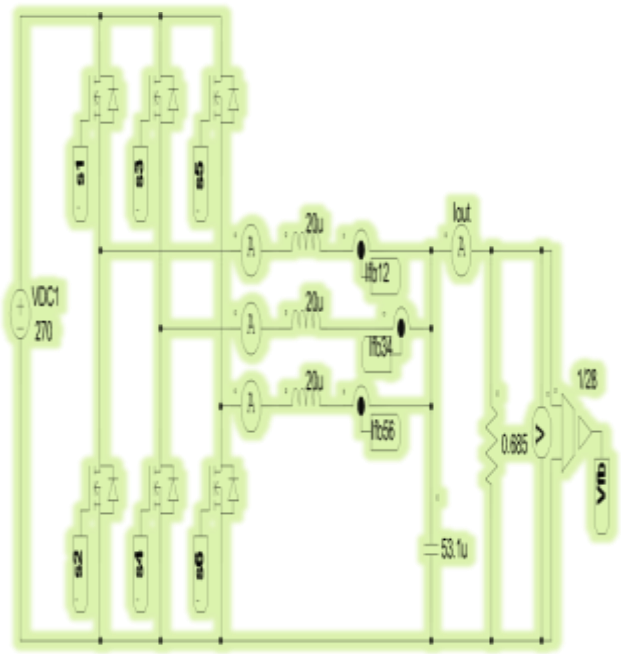


Figure. 2. The proposed circuit simulation model

The circuit's power stage is depicted in Figure 2. Each inductor is chosen for continuous conduction mode (CCM) with a maximum 12A DC peak-to-peak ripple (I). In addition, an output capacitor with a maximum voltage ripple of 3% is chosen. To use smaller passive components, a switching frequency of 100 kHz was chosen. The low-pass output filter, as shown in Figure 2, is made up of an inductor and a capacitor and

provides sufficient filtering (see Figure 4). This topology can also be used in discontinuous conduction mode (DCM) with a much smaller inductor value. This needs to be looked at further.

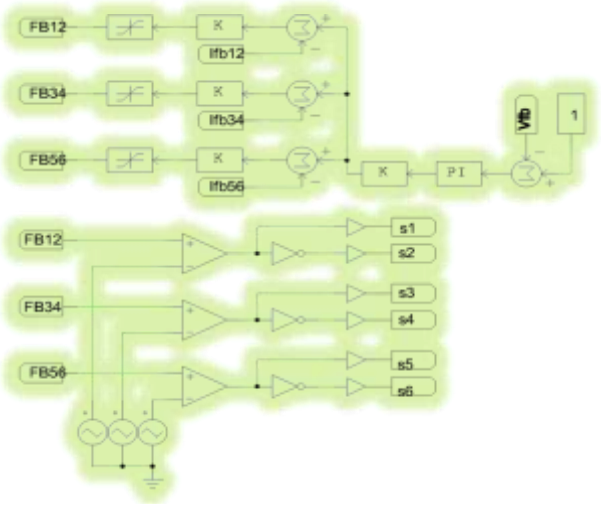


Figure. 3. Proposed circuit control and modulation scheme

High-quality waveforms and extremely stable voltage output are needed by avionic systems. Different approaches for control systems are proposed in the converter literature. There are two types of voltage control applications. The single loop voltage control [15-16] and the double loop voltage control [17-18] are the two types of voltage control.

Both interleaved systems were considered as one system during the design stage of the control system to protect one from the failure of the other. As a result, as shown in Figure 3, the control system employs three closed-loop PI controls with current feedback. The proportional-integrator controller system is a control method that compares the output to a reference signal using proportional and integrato methods. All K values are set to 1 in this controller, while P is set to 2 and I is set to 0.004. The voltage feedback is multiplied by 28 and the current feedback by 100. A double-loop control system is one that uses both voltage and current feedback loops. The voltage feedback comes from the system's output, which is directly connected to the load, as well as current feedback for each int. The control signals of switches 1-2, 3-4, and 5-6 are respectively the positive inputs of the comparators. Negative inputs are two-thirds phase difference triangular carrier signals at 100kHz. It is important to remember that even if a single interleaved stage fails, the desired output voltage can still be obtained using this control method.

VI. RESULTS

The waveforms of the converter output voltage (Vout) and current (Iout) are shown in Figure 4. The topology and simulations performed are in line with MIL-STD-704 [14]. In 0.02 seconds, the system output value reaches the appropriate value. At the output, there is also 0.1A of current ripple (Iripple) and 0.07V of voltage ripple (Vripple). With an output current of around 41A and a power output of 1150W, the conversion from 270V to 28V was completed. Table 2 lists the parameters obtained from simulations.

Table 2. Simulation Results.

Parameters	**Values**
VIN	270V
IIN	4.25A
VOUT	28V
IOUT	40.9A
VRIPPLE	0.07V
IRIPPLE	0.1A
Power	1145W

Outputs:

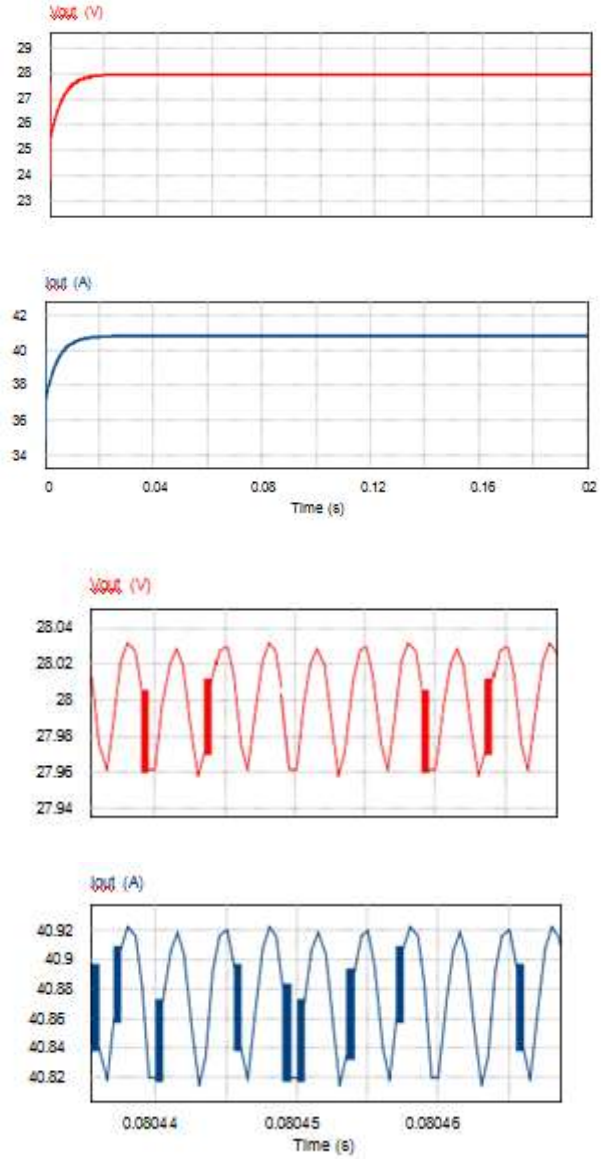


Figure. 4. Converter output voltage and current waveforms including ripples

Despite the fact that the converter device has a very high efficiency and almost no losses, the simulations conclude that all of the passive elements and semiconductors are perfect. Loss measurements, as well as thermal management and test results, will be needed in future work.

VII. CONCLUSIONS

For retrofit purposes, a 1.2kW synchronous interleaved buck converter was planned and simulated. The reliability, performance, and standards defined by MIL-STD-704F [14] are used to design the system.
To make the device interleaved, a high-frequency switch is used instead of a diode for the low side switch. This allows for optimal timing control and decreases the size of passive elements by allowing for a higher switching frequency, resulting in substantial reductions in losses. As a result of using synchronous and interleaved approaches when using SiC MOSFETs, the proposed topology has minimised losses and fluctuations. This also eliminates the need for thermal control. Furthermore, even if one of the interleaved stages fails, the necessary power output can still be obtained.

This topology, as well as its variations for various power levels, may be suitable for use in the aviation

industry. While the proposed converter achieves the desired loss reduction, further research is needed to conduct more comprehensive simulations and tests.

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