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A Electrical Behavior Of Total Ionizing Dose Impacts On Hfo2 And Al2o3 Gate Oxide Soi Finfet

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Abstract:

This study analyses how different gate oxides used in silicon on insulator (SOI) FinFETs are affected by total ionising radiation (TID). The device under consideration has a three-dimensional (3-D) SOI 30nm n-channel FinFET architecture with gate electrodes made of high-k hafnium oxide (HfO2) and aluminium oxide (Al2O3). Utilizing radiation-specific code for various gate oxides, 3-D simulations of the FinFET device were run in Visual TCADto examine the impact of TID on the device. The TID effects change the electrical characteristics, causing the device to deteriorate and the systems connected to it to fail.It has been discovered that the trapped charge density of oxide is more than that of interface. The leakage current and transconductance after irradiation rise as a result of TID. For both gate oxide materials, it has been found that the threshold voltage shifts as the ionising radiation exposure increases.

Keywords: insulator Silicon, total ionizing dose, fixed charge,FinFET, threshold voltage, interface charge,

INTRODUCTION

The usage of Silicon-On-Insulator (SOI) technology in commercial applications is growing in popularity. The use of numerous gate devices is a great way to meet ITRS requirements. Studying the radiation properties of the equipment utilised in nuclear settings and for space applications is therefore crucial. Therefore, since semiconductor technology is subjected to radiation of extremely high intensity, it requires careful consideration. One of themost noticeable effects on irradiation semiconductor technology is the total ionising dose effect. Incoming dose of radiation on the device causes device properties to deteriorate, according to well-documented studies.With the help of contemporary SOI and multi-gate technology, these degradations have decreased. In comparison to their bulk silicon equivalents, SOI devices have been demonstrated to be more radiationresistant overall [1]. They are less susceptible to the impacts of TID than bulk devices, though, and their reactionis more nuanced.The coupling effect between fins is said to be the cause. Additionally, it is demonstrated that irradiation weakens the degradation during the ensuing hot carrier test. Compared to OFF bias and transmission gate bias, the impact of irradiation on HCI is more clear with ON bias. One explanation is that it is thought that irradiation before the HCI test can break the Si-H bonds [2]. Studying the device's response to irradiation is crucial as new device innovations emerge. The implications of TID on a 30nm gate SOI FinFET are examined in this research. Radiation deteriorates the device's properties by affecting the buried oxide layer and thin gate oxide. As the radiation exposure is increased, certain device properties, like the ON current, voltage sources, leakage currents, and transconductance, alter.The device's geometry, manufacturing process, dose rate, biassing voltage, and post- irradiation temperature all have a significant impact on TID effects [3]. The TID phenomenonresults from the ongoing buildup of trapped energy in insulating levels and the formation of an inverted channel along the sidewall and top of the fins. Due to TID shocks, ultra-small SOI circuits show considerable changes in device properties.

II. MECHANISM OF RADIATION

Particle radiation and photon radiation are the two main categories of radiation. Charged particles like electrons, protons, ions, neutrons, and alpha particles make up particle radiation. A transistor or material produces extra carriers because particle energy also stimulates the ionisation process. Gamma () and x-rays make up photon radiation. Total ionising dose refers to the effects of radiation that relate with ionisation caused by rays. The radiation received by the material is used to calculate TID, which is expressed in [6].

` The creation of electron hole pairs in a radiation atmosphere is the main physical process that influences the device's characteristics. In electrolytic solution, 8.1 x 1012 pairs/cm3 of charged pair volume densities are generated per rad. Electrons are quickly swept out of the oxide within a few picoseconds due to their high mobility [4]. In those initial picoseconds, some electrons do however still reunite with the holes. The initial line frequency of the energy pairs created by the incident radiation and the strength of the electric field that separates the electron-hole pairs both have an impact on the recombination process. The distance between electron - hole pair and the line frequency are inversely related. This is also a factor of incident particle kind and energy and hence relies on linear energy transfer. The initial recombination-escaped holes are generally stationary and remain close to their point of formation, making them imprisoned[5]. The electrical properties of an irradiation FinFET device are influenced by thedevelopment of traps in the oxide layer, BOX, and interfacial traps at the corners of the fin.

Positive charges may become trapped, affecting the device under study's total mobility and voltage sources.

III. FINFET DEVICE DESCRIPTION

The mesh grid and 3D device modelling of an n-channel FinFET transistor were created using the Gds2mesh programme. Figure 1 depicts a three-dimensional model of a 30 nm n- channel Fully Depleted Silicon on Insulator (FDSOI) FinFET device that was shorted-gate (SG) modeled in Visual TCAD. In the nanoscale regime, this is a self-aligning technique that takes the place of traditional CMOS devices. The ITRS was utilised to determine the technology characteristics and supply volts for simulations of devices using the 30 nm node. According to ITRS specifications, the device structure has been optimised for a gate length ofthirty nm and an Ioff of one nanoampere [8]. Gate tunnelling leakage, the hot electron effect, and DIBL all act as limiting factors on the scaling of gate oxide thickness. Therefore, a high- dielectric like hafnium oxide is used to substitute silicon dioxide (SiO2) in order to get over these constraints (HfO2). Where a gate built of the high-dielectric hafnium oxide (HfO2) (k=22) surrounds the device's n-type body, which has dimensions of height Hfin and thickness Tfin [7]. The distance between the gate and the channel is widened by the high-gate dielectric while the threshold voltage is held constant. This is accomplished without raising gate capacitance. Using the following formula from the equation, the effective EOT (Tox) value of 1 nm is determined.

IV. RESULT AND DISCUSSION

At room temp, current-voltage parameters were measured both before and after gamma radiation exposure. Aluminum oxide Al2O3 (k = 8.3) and hafnium oxide HfO2 (k = 23) were used as the gate oxide materials for the simulations. In every instance, the TD was adjusted instages from 100krad to 1M while the dose rate was held constant at 10rad/s. Measured, analysed, and reported adjustments were made to the Id-Vgs features, voltage sources, conductivity, oxide stranded charge concentrations, and contact trapped charged concentrations.

4.1 Id-Vgs Characteristics

At room temp, current-voltage parameters were measured both before and after gamma radiation exposure. Aluminum oxide Al2O3 (k = 9.3) and hafnium oxide HfO2 (k = 22) were used as the gate oxide materials for the simulations. Every time, the total dose was raised gradually from 200 krad to 2M while the dose rate remained constant at 11 rad/s. Measured, analysed, and reported adjustments were made to the Id-Vgs features, voltage sources, conductivity, oxide stranded charge concentrations, and contact trapped charged concentrations.

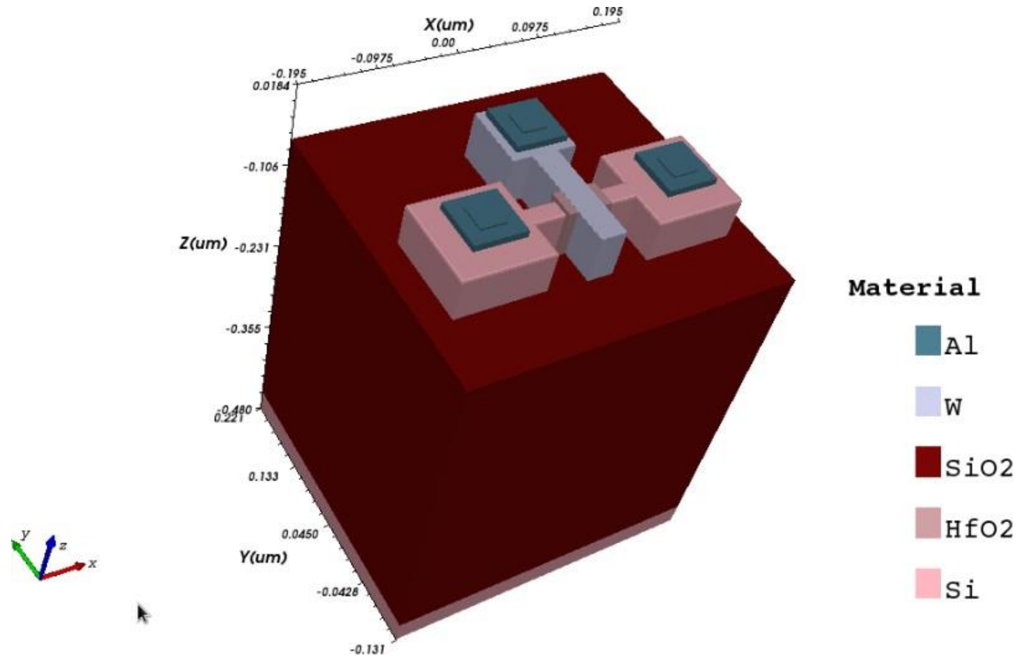
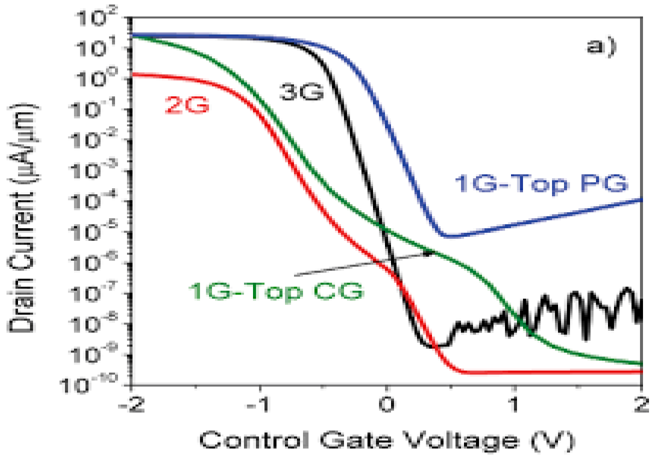


Figure 1 The high-k 30nm schematic as seen in visual TCAD

Some of the positively charged holes slowly disperse toward the Si/SiO2 boundary, where deep hole traps contain them. Radiation-induced electron-hole pairs undergo recombination right away and cannot be used for further radiation effects. This has a big effect on how well the thing works. The threshold voltage changes as a result of trapped charges brought on by radiation that build up in the gate oxide. Figure 2 displays the Id-Vgs curves for the gate oxide materials made of HfO2 and Al2O3 in both unprocessed and gamma-irradiated devices.



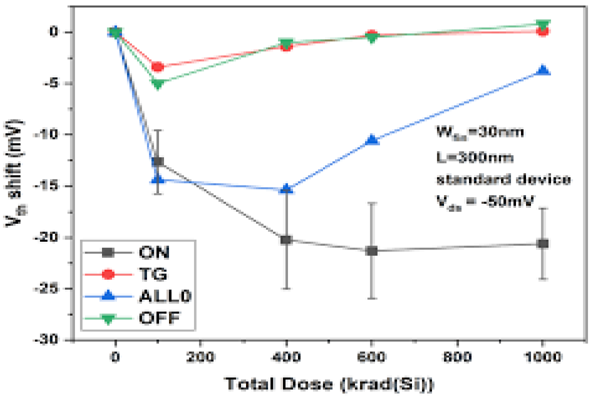
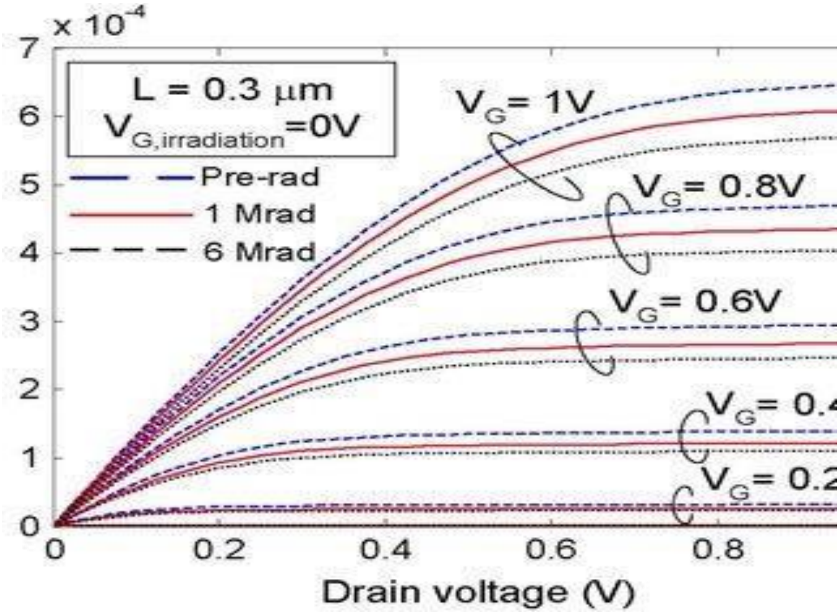


Figure 2 Id-Vgs characteristics for (a) HfO2 and (b) Al2O3 gate oxide materials in a30nm n channel SOI FinFET device at Vds = 50mV.

Transconductance (gm), that is closely related to drain current, is a significant analogue performance metric of FinFET devices. Peak method simply in the n-channel is determined by the velocity of the carriers [9]. As a result of irradiation, the channel's carriers disperse, lowering transconductance. Transconductance rises with an increase in overall dose rate up tothe peak value, as seen in Fig. 3.

The lines often start to converge after the gadget enters conduction. The 30nm n-channel SOI FinFET device's threshold voltage was discovered to be 234.78 mV and 240.67 mV for the gate oxide materials of HfO2 and Al2O3, respectively. The threshold value for the irradiated gadget shifts to 188.52 mV and 194.30 mV when it is subjected to a 1 Mrad gamma dosage.It can be seen from Fig. 4 that the change in peak value is caused by an accumulation of trapped ions at the contact and in the oxide[10]. Al2O3 has a greater absolute threshold reference voltage than HfO2, yet HfO2 has a bigger change in sub - threshold shift.As a result, device engineers should design their devices to stop the threshold voltage from shiftingfor a greater dose rate. For virgin and irradiated 30nm FinFET devices, the values are presented in Table 1 for electrical characteristics and threshold voltages shift for HfO2 than Al2O3 gate oxide.



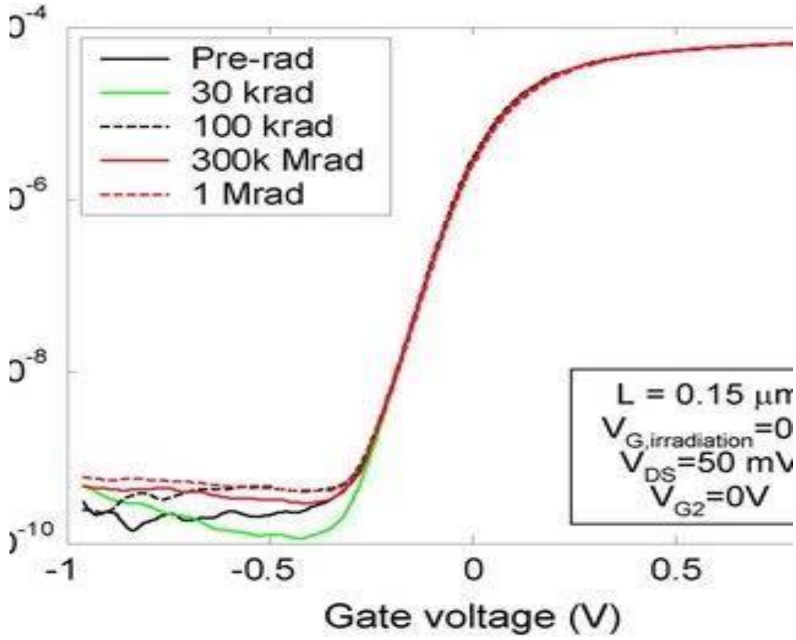
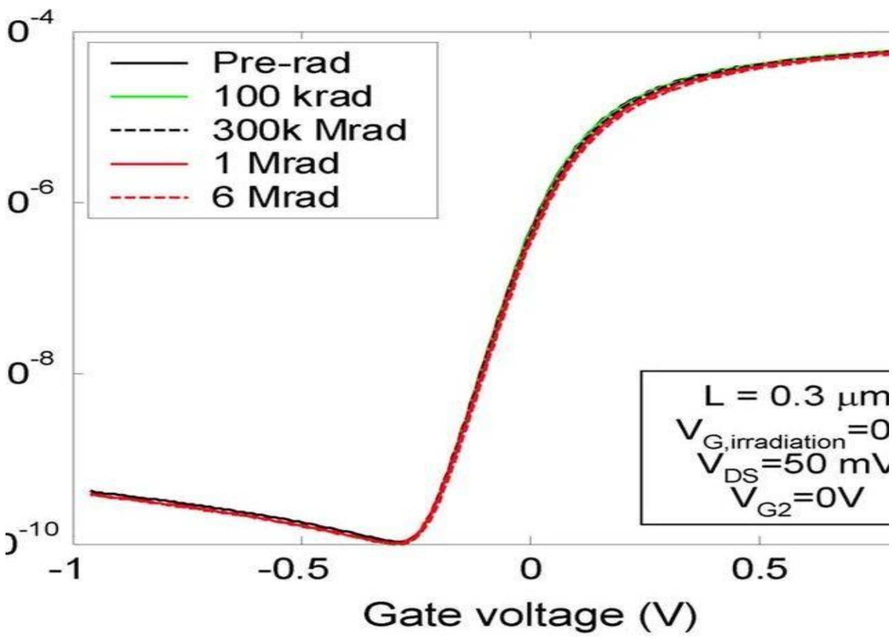


Figure 3Transconductance of a 30 nm n channel SOI FinFET device with gamma radiation for (a) gate oxides made of HfO2 and (b) gate oxides made of Al2O3 at Vds =50 mV.

4.2 Oxide and Interface Trapped Charges Density

The threshold voltage change caused by trapped charges at the interface and in the oxide, as seen in Fig. 5, has been explained in the previous section. Charge is trapped by ionising radiation in dielectrics. It is obvious that the oxide positive charge is higher than the interface charge distribution, leading to a dominant voltage shift caused by trapped oxide charges.



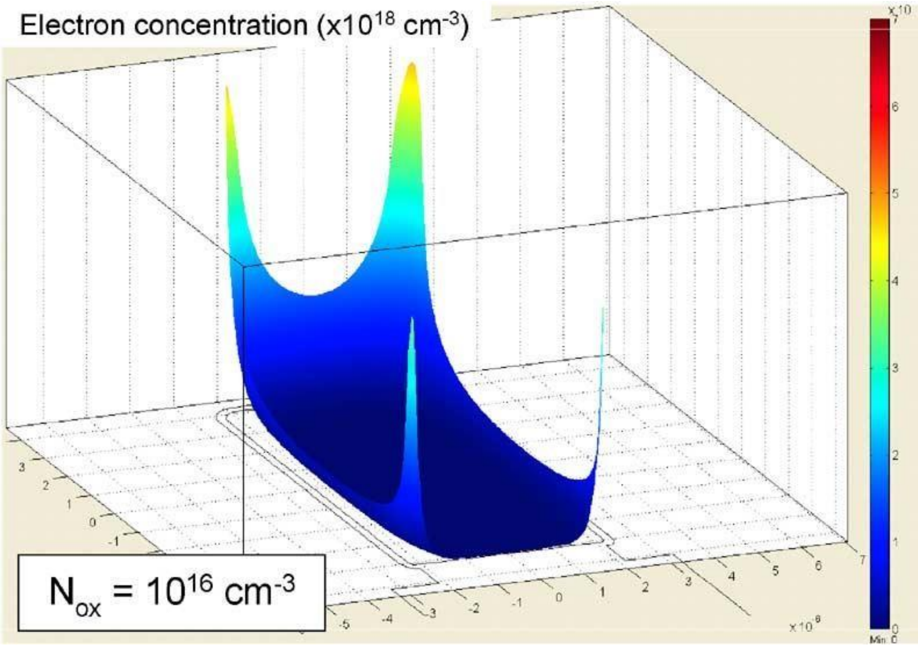


Figure 5 (a) Interface and (b) Oxide trapped charge density

V. CONCLUSION

The TID impact altered the device's numerous performance metrics. The major cause of a gamma-irradiated device's deterioration is a rise in trapped charge distribution. It was discovered that the oxide imprisoned energy was greater than the interface trapped charge. It was found that when radiation doses rise, greater degradation is caused and the voltage level for the treated FinFET device drastically dropped. HfO2 gate oxide materials have a larger shift in threshold voltage than Al2O3 gate oxide elements. This strongly implies that when exposed to radiation, Al2O3 performs better than HfO2 as a dielectric for use in gate oxides. The TID influence drastically reduces the gadget's performance.

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